OVERVIEW

The **TS-POE100** is a PC/104 peripheral board (standard format) that provides a 10/100 Ethernet port integrated with a Power-over-Ethernet splitter circuit, which is capable to provide up to 12W of power through the PC/104 bus.

The TS-POE100 is compatible with both Technologic Systems x86 and ARM single board computers. **TS-POE100** features includes:

- ✔ Power-over-Ethernet Splitter
- ✔ Integrated 10/100 Ethernet Port
- ✔ 2.4 amp @ 5V (12W)
- ✔ Provides regulated 5VDC to SBCs through PC/104 connector
- ✔ Jumper selectable I/O and IRQ
- ✔ Isolated power
- ✔ PC/104 Dimensions 3.6 x 3.8 inches
- ✔ Wake-on-LAN integrated with PoE
- ✔ Programmable sleep modes
- ✔ Linux driver and utilities available
- ✔ RoHS compliant (Restriction of Certain Hazardous Substances)

The **TS-POE100** features a Linear Technology LTC4267 PoE chip fully compatible with the IEEE 802.3af specification. The TS-POE100 is a Power-over-Ethernet splitter interface that provides up to 12W (2.4A @ 5V) to external devices (class 3 devices). The internal switching-regulator delivers regulated 5VDC to the PC/104 connector, enabling a complete stackable SBC system to be powered.

In addition, the **TS-POE100** provides an integrated 10/100 ethernet port through the ASIX AX88796B embedded MAC with on-chip PHY. It interfaces with the PC/104 connector via 16-bit data bus and the register map is NE2000 compatible. The ASIX solution features Wake-on-LAN functionality, enabling the Ethernet chip to enter in sleep mode with programmed wake-up on the reception of a magic network package. Once integrated with the PoE, this function allows a complete SBC system to enter power-save mode and to wake-up through the network whenever wanted.

PRODUCT VIEW
HARDWARE CONFIGURATION

The **TS-POE100** jumpers select one-of-three IRQ lines and one-of-four I/O address regions. Also, it is possible to do PC/104 16-bit access using only the 64-pin PC/104 connector in ARM mode if the ARM jumper is ON. Jumpers IRQ5, IRQ6 and IRQ7 selects the desired ISA IRQ line for the TS-POE100 MAC.

**I/O ADDRESS**

The PLD and MAC I/O address locations can be configured using jumpers Add1 and Add2 according to the table below:

| Jumper settings for I/O address space selection |
|-------|-----------------|---------|---------|
| PLD I/O | MAC I/O | Add1 | Add2 |
| 0x100  | 0x200  | OFF  | OFF  |
| 0x110  | 0x240  | ON   | OFF  |
| 0x120  | 0x300  | OFF  | ON   |
| 0x130  | 0x340  | ON   | ON   |

**BASE REGISTER MAP**

The **TS-POE100** has 4 registers of 4-bits each which appear implemented on the PLD.

<table>
<thead>
<tr>
<th>I/O Addr</th>
<th>Description</th>
<th>Data Access</th>
<th>Bits and such</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base+0x0</td>
<td>Board identifier</td>
<td>Read only</td>
<td>returns 0x5 unique ID to verify presence</td>
</tr>
<tr>
<td>Base+0x4</td>
<td>PLD revision</td>
<td>Read only</td>
<td>Returns PLD revision</td>
</tr>
<tr>
<td>Base+0x8</td>
<td>SRAM control register</td>
<td>Read only</td>
<td>bit 3 = IRQ7 jumper status (1=ON, 0=OFF)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit 2 = IRQ6 jumper status (1=ON, 0=OFF)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit 1 = IRQ5 jumper status (1=ON, 0=OFF)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit 0 = ARM jumper status (1=ON, 0=OFF)</td>
</tr>
<tr>
<td>Base+0xC</td>
<td>Power control</td>
<td>Bit 0 is RW</td>
<td>bit 3:1 = reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit 0 = 5VDC power to PC/104 bus control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(1=power ON, 0=power OFF)</td>
</tr>
</tbody>
</table>

For a complete description of the MAC register map (which is NE2000 compatible), please refer to the ASIX AX88796B documentation.

**POWER INPUT AND ASSEMBLY**

In order to power up a system including a PC/104 computer and a TS-POE100, the only required cable/connection is the POE ethernet cable, which must include network signals and power. Connect it to the TS-POE100 RJ45 connector.

Power can be either on the spare pairs or on the data pairs of the 8-lines network cable. The power level that should be found at the network cable is 48VDC @ 0.35A. If the TS-POE100 detects valid POE signature and classification stages, it will transmit regulated 5VDC to the PC/104 bus, powering up the other boards (peripherals and computers) connected to it.

The on-board green LED named LED 5V will come on in case the TS-POE100 detects a valid POE power source. Also, there are on-board LEDs for the MAC - Link and Network Activity.

The TS-POE100 can provide up to 12W of power (2.4Amp @ 5VDC) – this is Class 3 POE implementation.
SOFTWARE SUPPORT

The register map of ASIX AX88796B ethernet chip is NE2000 compatible, so driver support is straight-forward.

Technologic Systems provides a Linux driver suitable for both Kernel versions 2.4 and 2.6. The Linux driver provided detects jumper selection, automatically configuring IRQ and IO parameters. In case one needs to skip this feature, the “mem” and “irq” parameters are available to setup IO base address and IRQ line, respectively.

```
# insmod -f /lib/modules/2.4.4.26-ts11/kernel/drivers/net/tspoe100.o
# ifconfig eth1 down
# ifconfig eth1 up <IP>
# add route default gateway <IP> eth1
```

In addition, Technologic Systems provides Linux tools to manage the sleep-mode and Wake-on-LAN functions. Tools for programming the MAC address are also provided. Contact Technologic Systems for further information regarding software support for the TS-POE100.

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