TS-7990

This board can drive one of three LCD panels

BOM Issues:

CPU (U4) can be Quad or Single Core
RAM (U22, U23) is always 4 Gigabit Ind. size
WiFi option = K1 and R34
R36 populated to indicate quad core CPU
Accellerometer option = U21
SATA Caps C139 thu C142 not pop in std BOM
CH1, R33, R35, R37 not populated in std BOMs

Res. Straps:

R151 thru R153 are pop for LXD LCD
R34 is pop for WiFi
R35 is pop for 512MB RAM
R36 is pop for Quad core
R37 is pop for Comm Temp Single
R33 is not pop for now

LXD LCD version

R151 thru R153 pop.
CN1 and CN5 pop.
CN8 and CN9 not pop.
R170-R177, J1, and HD6 not pop.

PCIe socket Option:

CN13 = SIM socket
J3 = Mini-PCIe socket
U45 = 100 MHz clock chip
MT5 and MT6 = PEM standoffs

MT LCD version

R151 thru R153 not pop.
CN1 and CN5 not pop.
CN8 and CN9 pop.

Remote LCD Option:

R170-R177, J1, and HD6

CN1 can not be pop for this option

SATA or PCIe

C139-C142 populated for SATA

OR

C295-C298 populated for PCIe

3 Production BOMs - Oct. 2015

#1 = Base model for MT LCD

Single Core CPU - I Temp
CH1, R33, R35, R37 not pop
C139 thru C142 not pop.
U21 and K1 not pop
R34, R36 are not pop
R151 thru R153, CN1 and CN5 not pop.
Remote LCD parts are pop.

#2 = Base model for LXD LCD

Single Core CPU - I Temp
CH1, R33, R35, R37 not pop
C139 thru C142 not pop.
U21 and K1 not pop
R34, R36 are not pop
R170-R177, J1, and HD6 not pop.

#3 = Dev Kit model = LXD LCD

Quad Core CPU
CH1, R33, R35, R37 not pop
C139 thru C142 not pop.
R170-R177, J1, and HD6 not pop.

If we need Dev Kit for MT LCD
Then we must swap out LCD conn.

If we need SATA, must swap caps

If we need remote LCD
Then must add Remote parts

FPD-Link = 7-bits per clock prototcol

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Rev.P1 Problems:

- ✓ Correct 100 uF cap decal
- ✓ Add Okaya Detect like 7690
- ✓ Change to new Back Light Reg that can do 30V
- ✓ Q6 has bad decal ? See Q8 on 7680
- ✓ LXD main conn needs moved 1 mm south
- ✓ LXD Touch conn. needs moved south 3 mm
- ✓ Change SPI Flash (U32) to SOIC
- ✓ U37 should be powered by 3.3V
- ✓ Fix R79 - 14.7K is wrong
- ✓ P4 is interfering with COM2 header
- ✓ Remove R155, 156 and [GPS ?]
- ✓ Add RJ45 for Remote LVDS
- ✓ Change USB concole and OTG to Type B vert.
- ✓ Change RTC to ST Micro
- ✓ C73 and C74 are on wrong pair
- ✓ Add 2x7 header for remote LCD
  3- 5V, 3- GND, 4- SPI/I2C, 1- En Pwr, IRQ, PWM

Bigger 5V Reg ?

4 mm keepout around CPU

Add HDMI ?

Try to lower cost of USB device connectors

All 4 iMX6 UARTs MUXed thru FPGA

FPGA will have 2 MAX3100 UARTs

Features that require UART:

4 RS-232 Ports
3 RS-485 Ports
1 TTL UART to DC
1 UART for BlueTooth

Heat Sink for CPU

CTS # APF19-19-13CB/A01
CTS # APF19-19-10CB/A01
CTS # APF19-19-06CB/A01

Rev.A problems:

R111 should have a 7.5 ohm in parallel
or change value lower

Add 4mm keep-out around CPU

Allow software to select LCD 16/20V
This will minimize BOM stock

Backlight is bad - must drive EN pin off

RS-232 problem causes no boot
must add 2K resitor across 5V switch ?

D5 anode to wrong side of coil
Must remove Q5 for short term fix

Res. Touch wrong IRQ polarity - Q11

Add Reg_5V to CN99

DC for 15 second Power Hold

This requires 4 SiLab A/D chan
SuperCap1_V, SuperCap2_V
Chrg_V, and V_Internal

One SiLab PWM output to set Charge current

1 SiLab DIO - not sure if needed

One FPGA pin for Power Fail signal

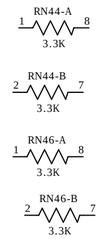
Prototype Build:

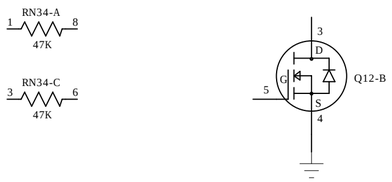
Include:

Accelometer (U21)
Mini-PCIe connector (J3, CN13, PIMs, and U45)
No GPS (K2)
WiFi (K1) only on Quad core

Build 3 Quad core with 1 GB RAM with CN1 and SATA Caps
Build 3 Single Core with 1 GB RAM with CN1 and PCIe caps
Build 3 Single Core with 512 MB RAM with CN8 and PCIe caps

CH1, R33, R35, R37 not populated





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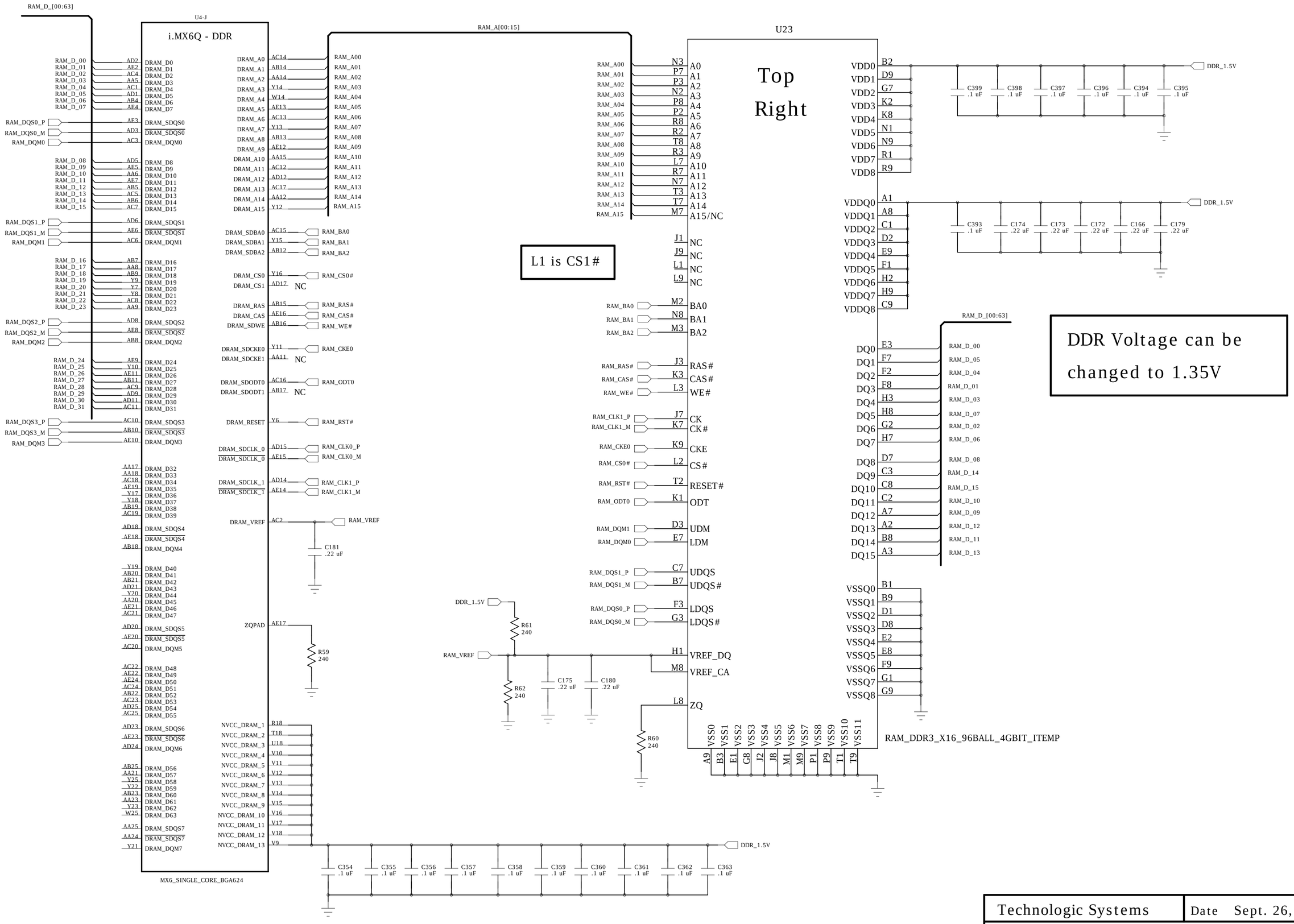
RAM_D_[00:63]
U4-J
i.MX6Q - DDR
RAM_A[00:15]
U23
Top
Right
L1 is CS1#
DDR Voltage can be changed to 1.35V
RAM_DDR3_X16_96BALL_4GBIT_ITEMP
MX6_SINGLE_CORE_BGA624
DDR_1.5V
VREF
NC
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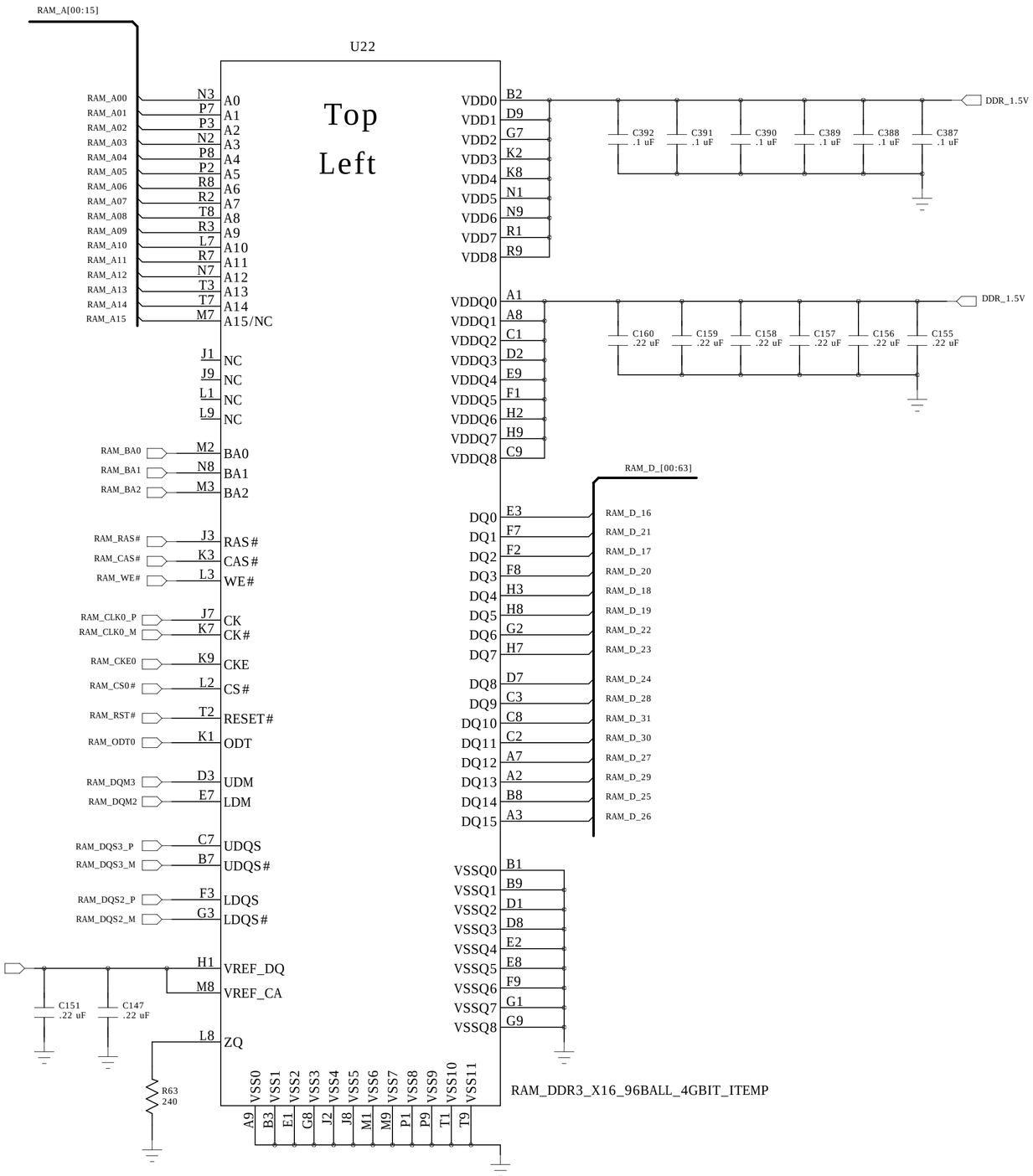
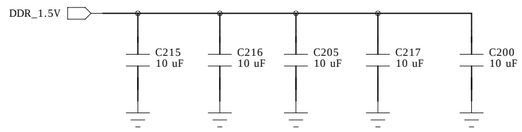
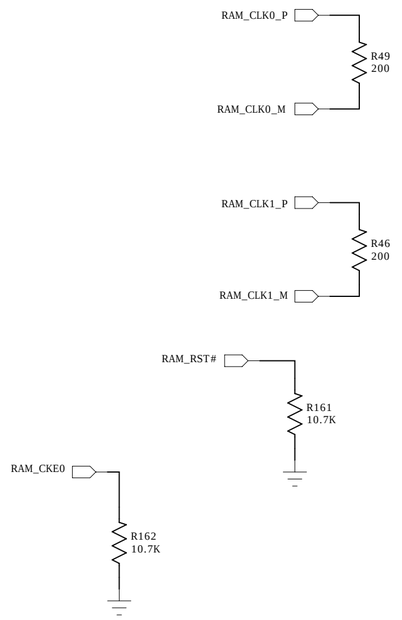
RAM Data bits 16-31

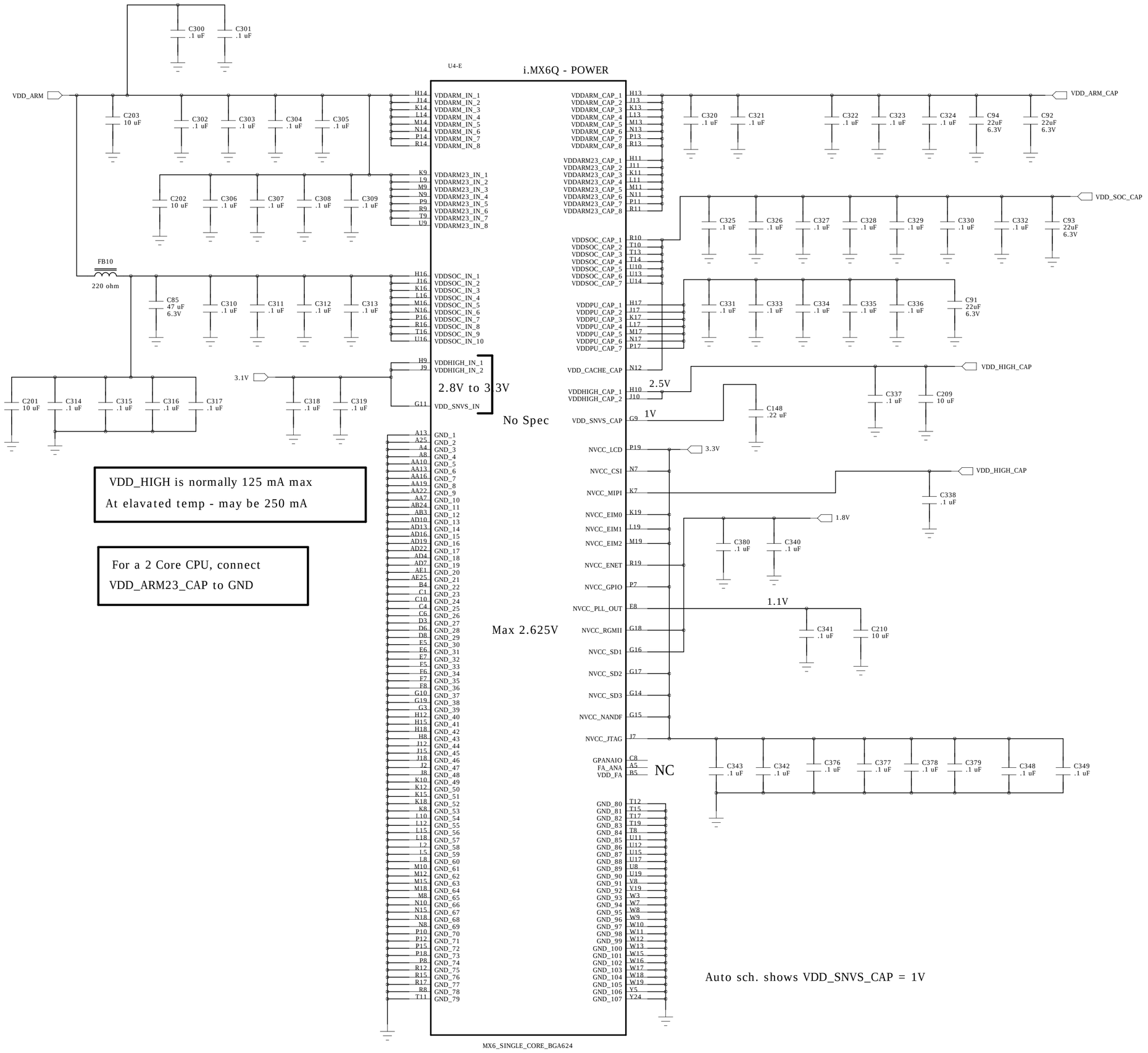






Very odd
RAM clock pair terminated
with 200 ohm resistors

iMX6 Power Pins



VDD_HIGH is normally 125 mA max

At elavated temp - may be 250 mA

For a 2 Core CPU, connect VDD_ARM23_CAP to GND

Data Sheet says

Power Sequence

VDD_SNVS_IN = 0 - must be first

VDD_ARM_IN = 1

VDD_SOC_IN = 1

VDD_HIGH_IN = 2

NVCC_DRAM = 3

DRAM_VREF = 3

NVCC_RGMII = 3

NVCC_xxxx = 5

- EIM0,1,2
- ENET
- GPIO
- LCD
- NAND
- SD1,2
- SD3
- JTAG

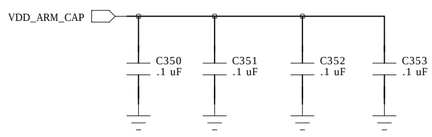
Note: VDD_HIGH_IN can be shorted to VDD_SNVS_IN

Page 21 of "Auto" schematic says

"External LDO no longer needed for PLL"

"MX6 was fixed"

Smart Dev sch Page 20 also says not needed



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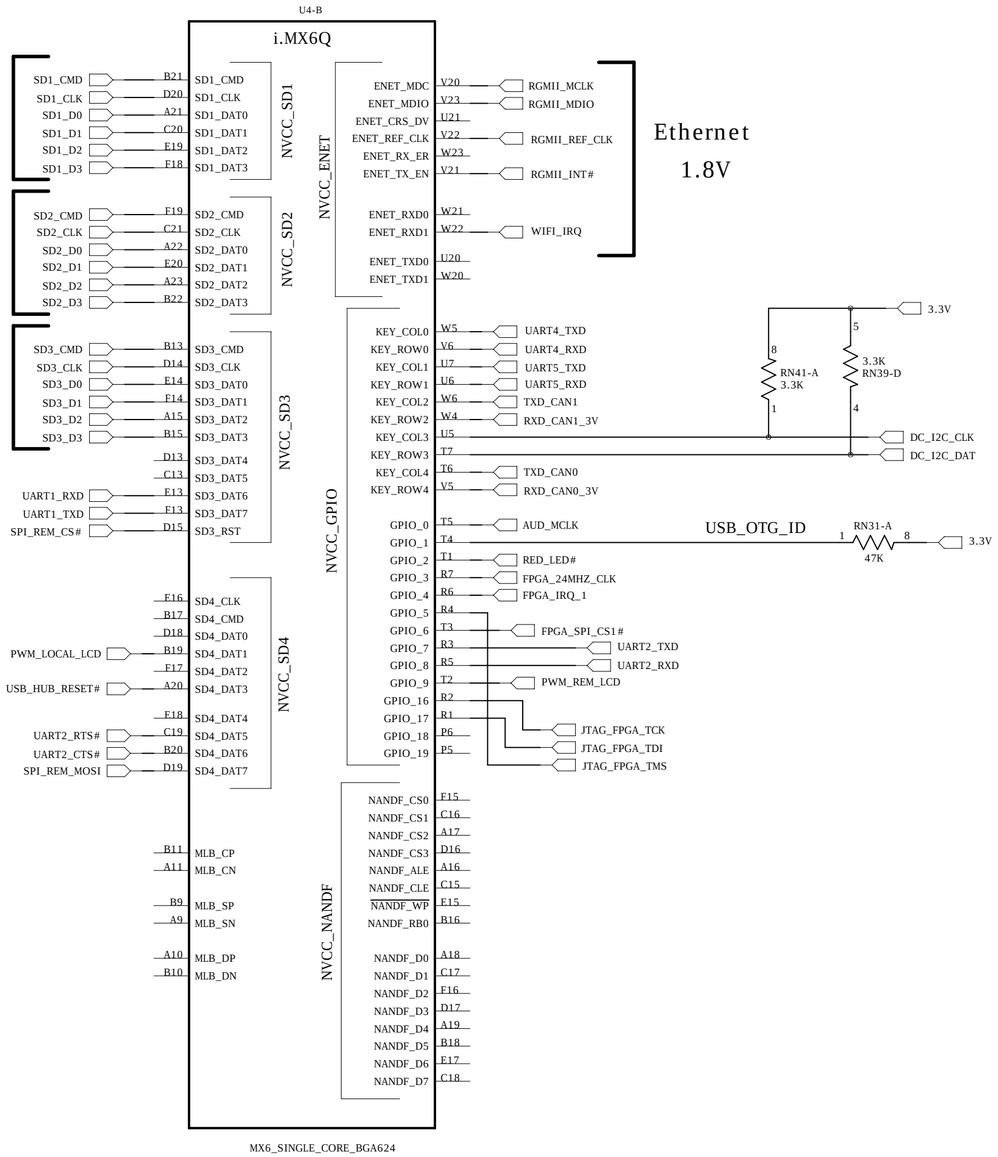
SD, GPIO, NAND

WiFi (1.8V)

SD Card (3.3V)

eMMC (3.3V)



Ball B19 is PWM on 4900

Balls T2 and T4
can also be PWM

4 PWM total

PWM on SD4_DAT 1 or 2
GPIO_1 and GPIO_9

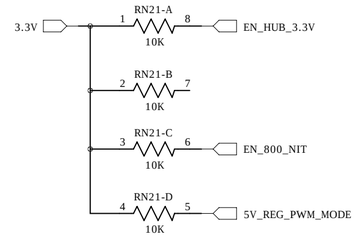
TS-7970 changed CPU pins:

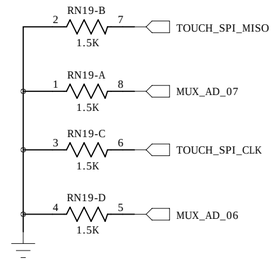
FPGA_SPI_CS#

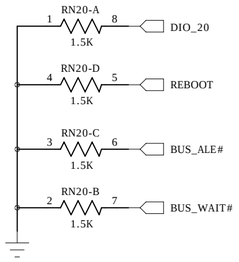
FPGA_RESET#

UART4_CTS#

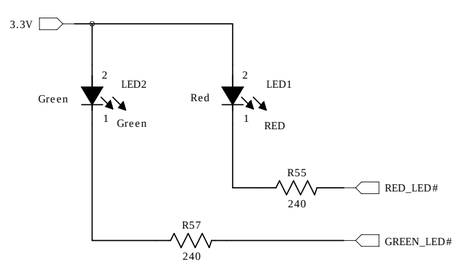
Bias Res.







iMX6 LEDs



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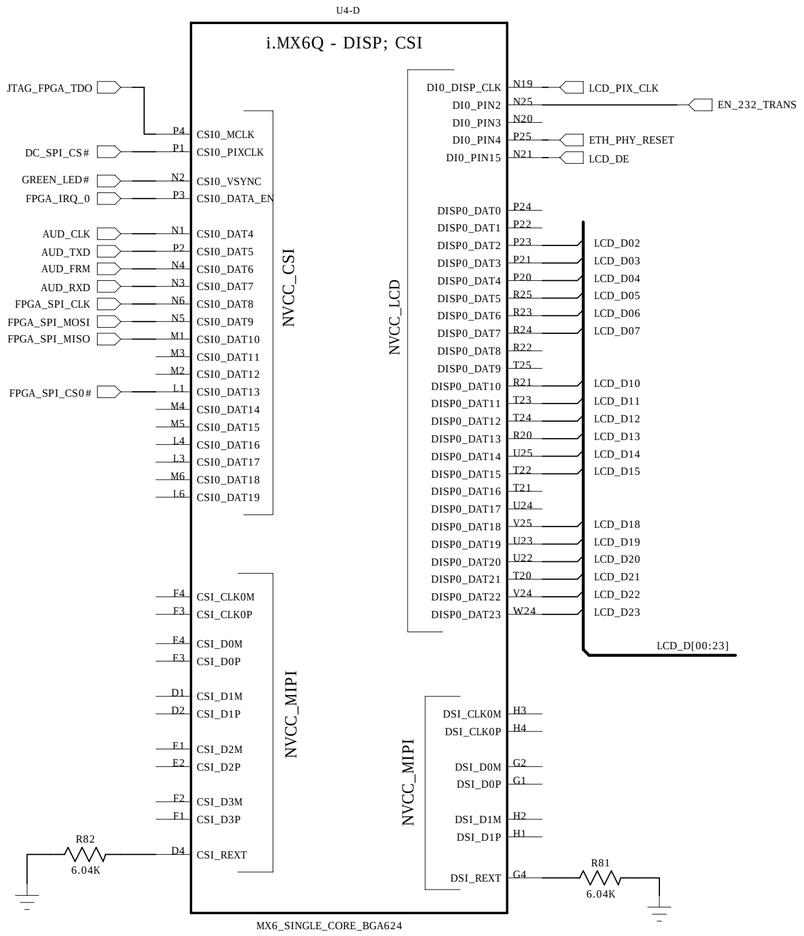
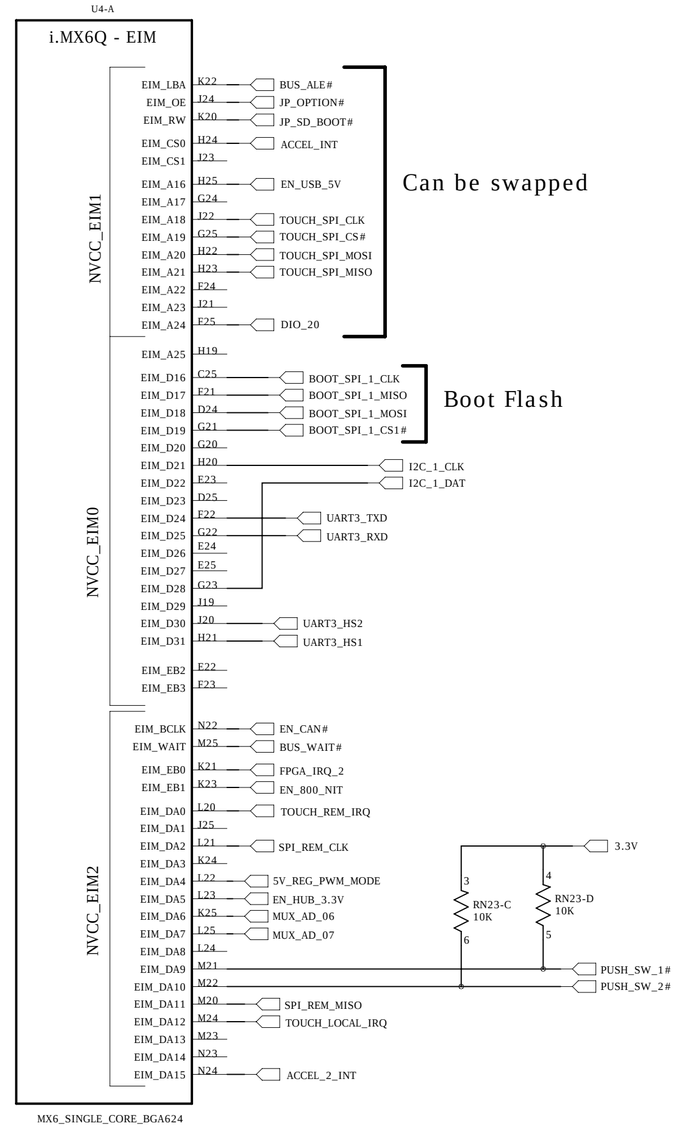
LCD



EIM



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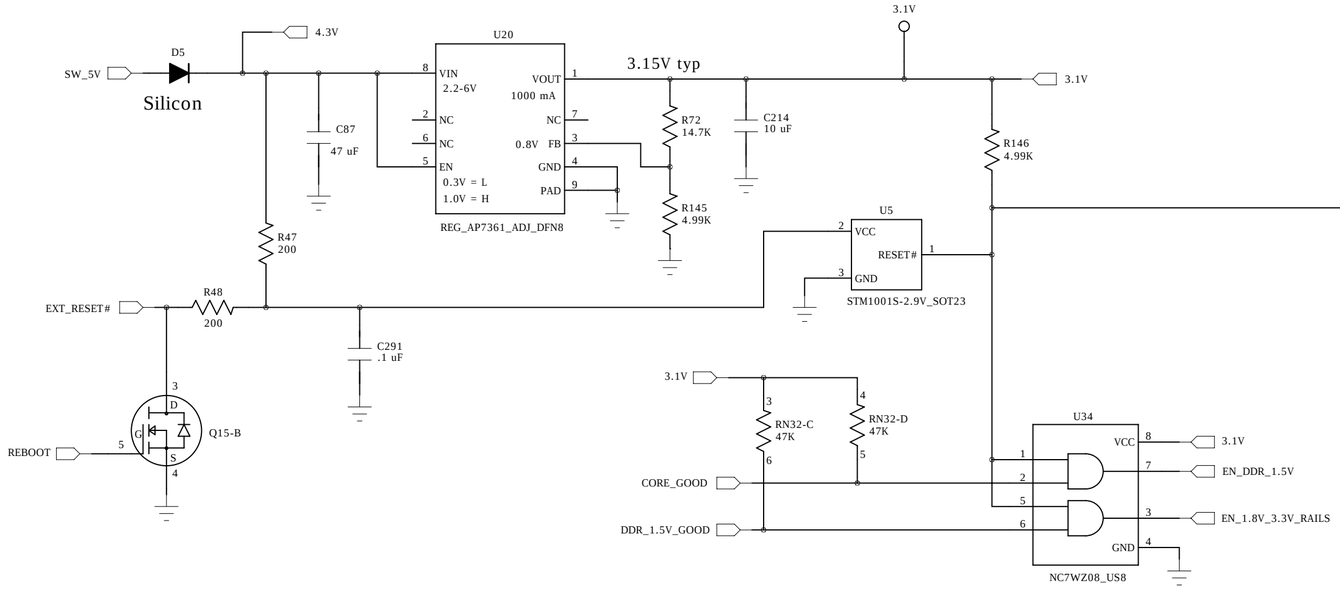
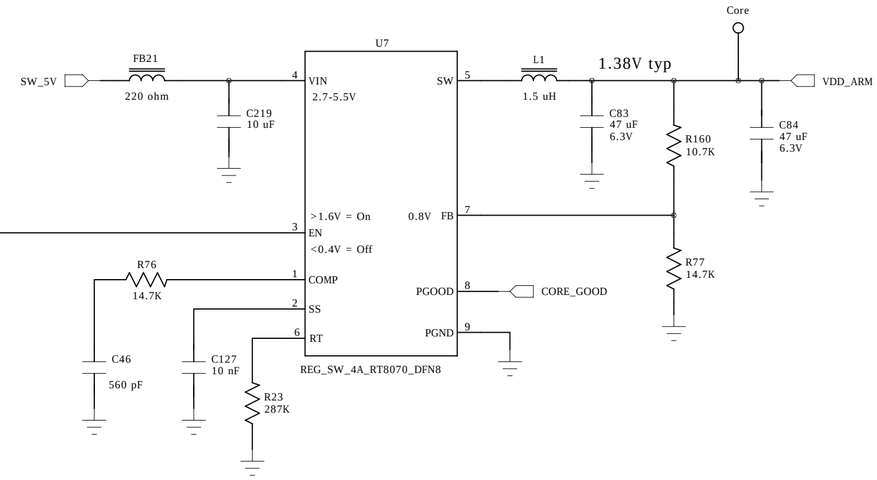
Power Supplies

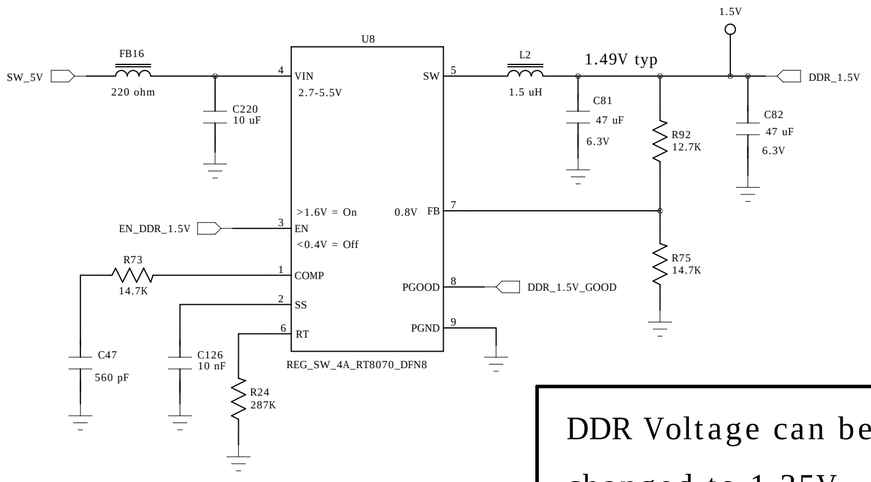
Linear 3.1V Reg. #1



ARM Core Rail #2

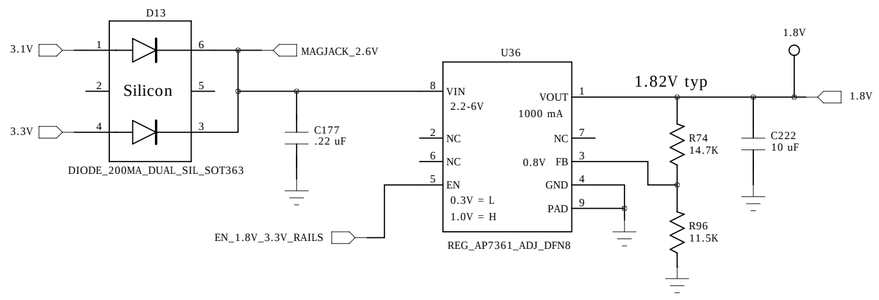


DDR3 Reg. #3



DDR Voltage can be changed to 1.35V

Linear 1.8V Reg. #4



For Eth PHY and WiFi/Bluetooth

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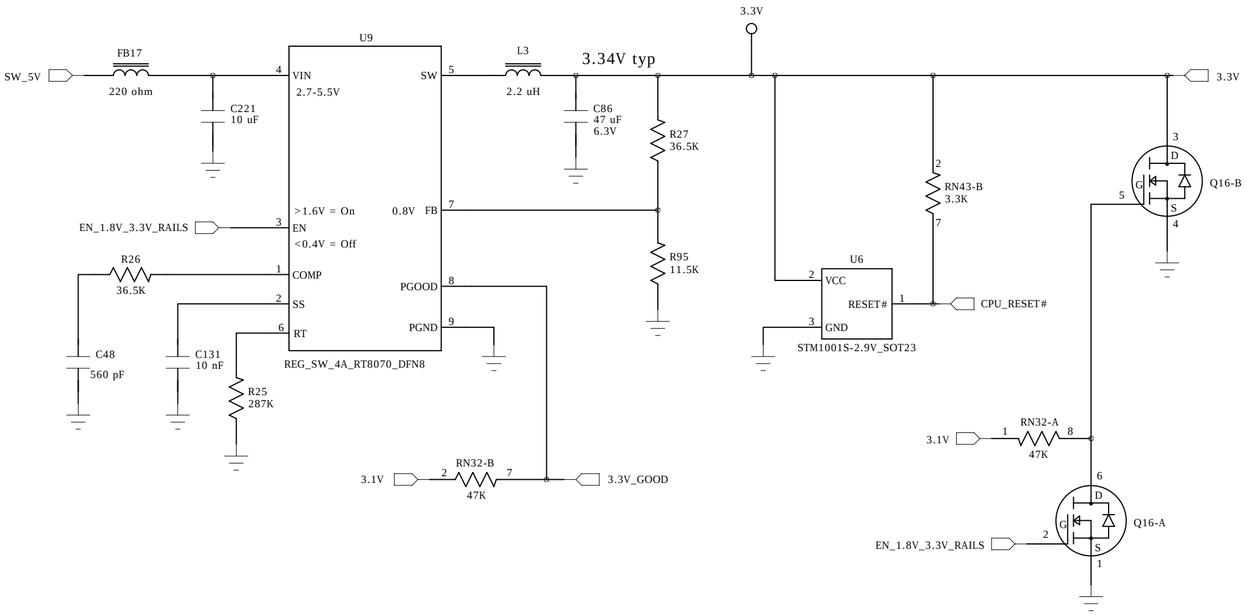
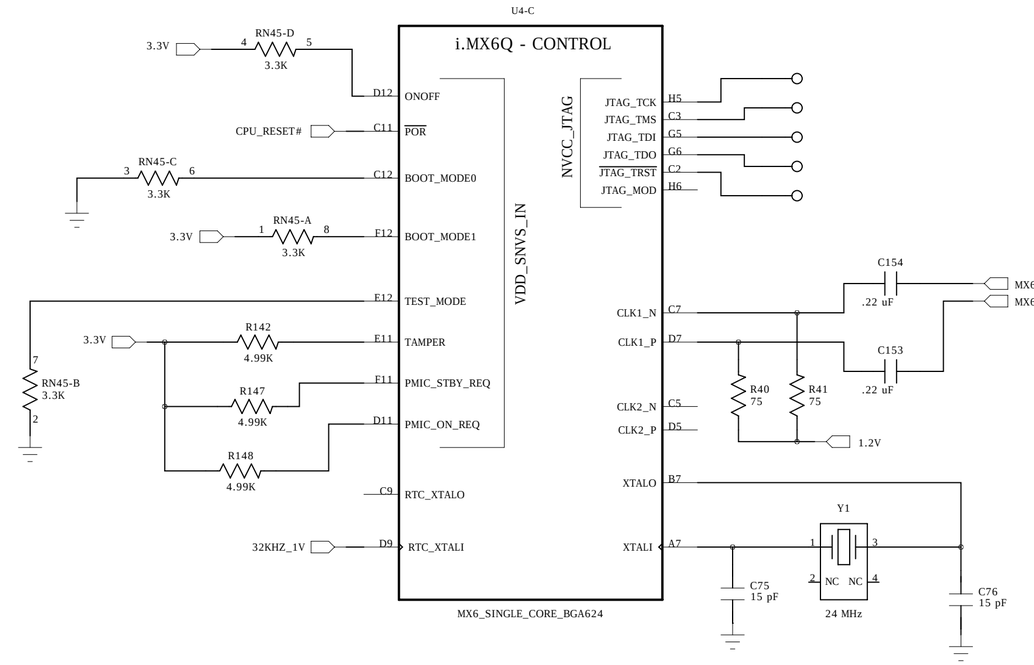
3.3V Reg. #5

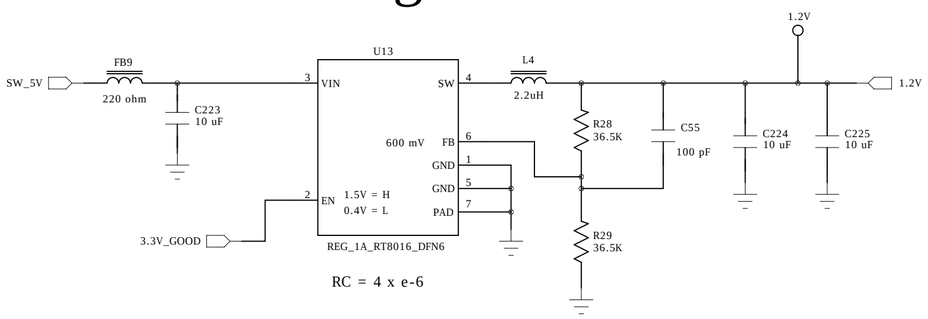


CPU Control



Errata - slow start up - 2ms

1.2V Reg. #6



For Eth. PHY Core and CPU

BOOT_MODE

MSB LSB

0 0 = Fuses

0 1 = USB

1 0 = Internal Boot

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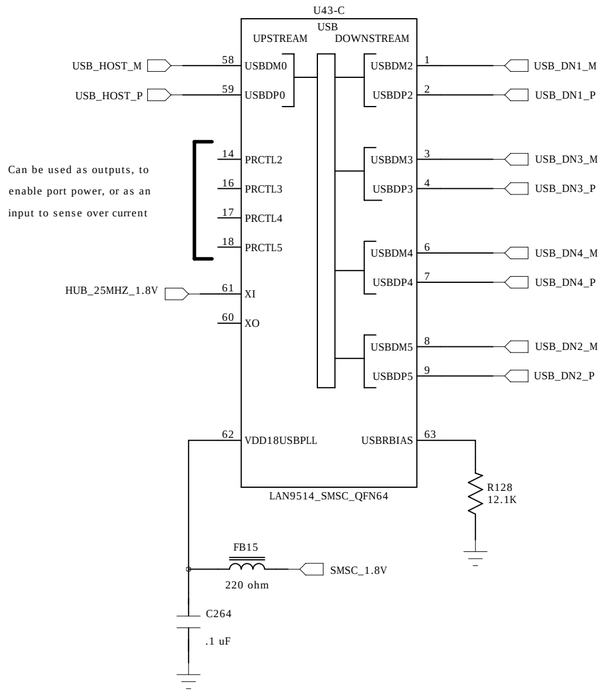
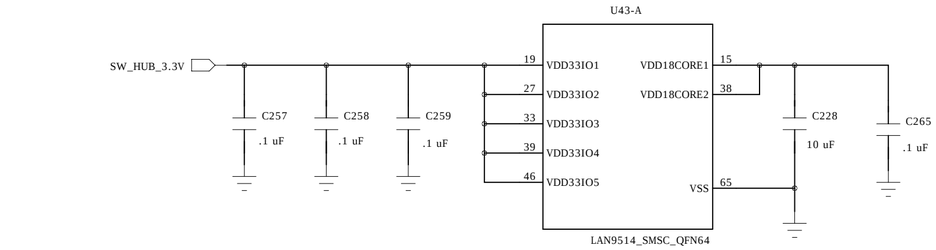
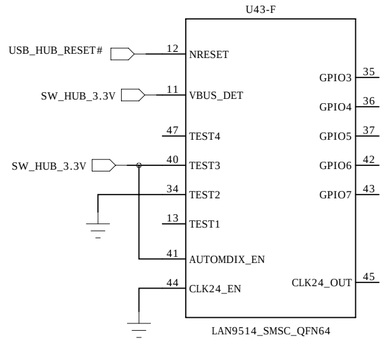
2nd Ethernet Port

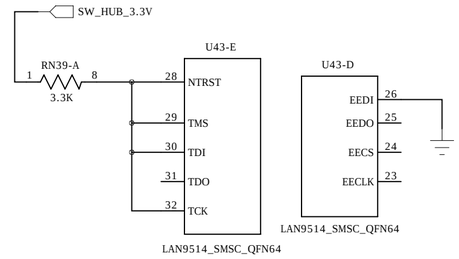
Typical 3.3V current with all ports active is 288 mA (950 mw)

SMSC USB Hub

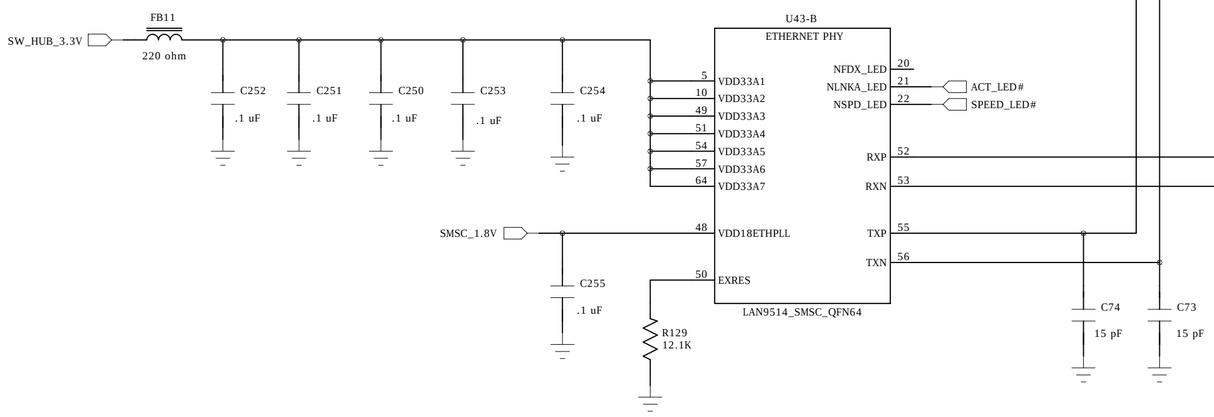








SMSC Ethernet Port



Vert. MagJack

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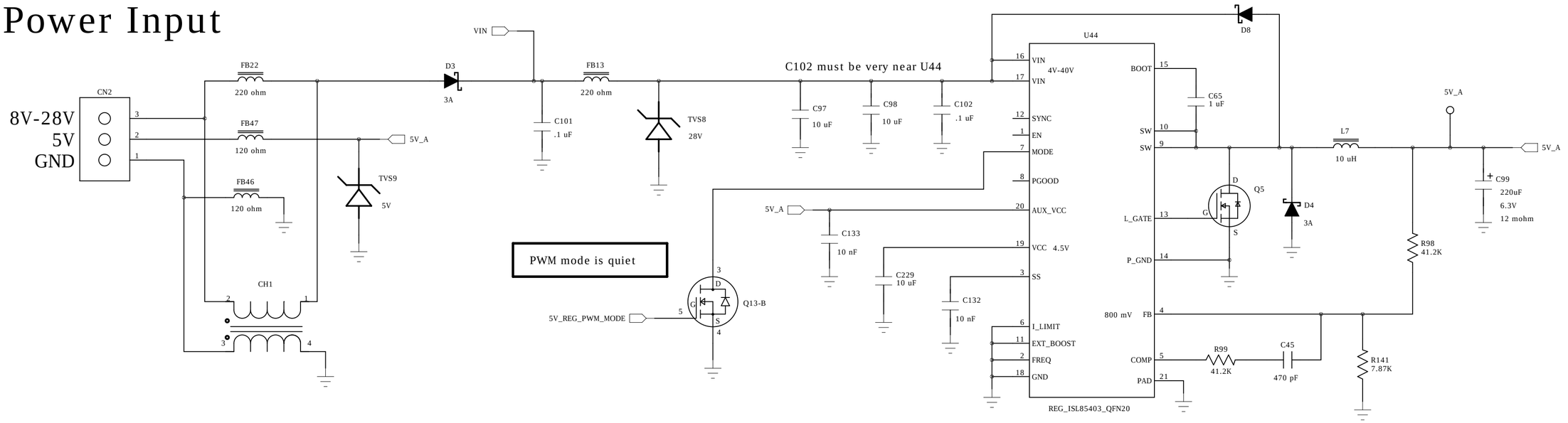
5V Power Supply (2500 mA)

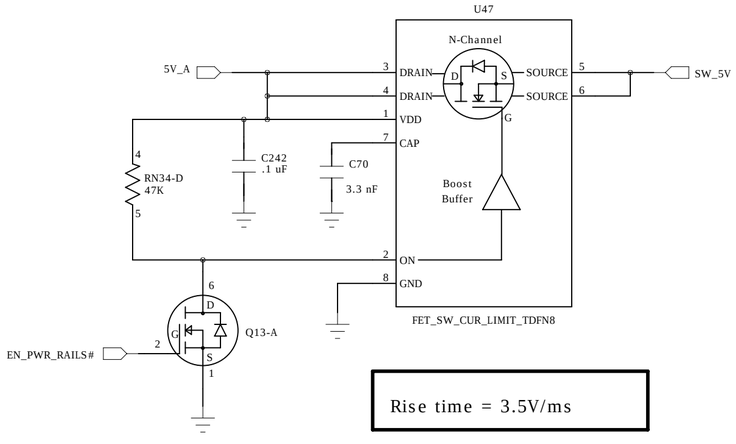
Power Input



.063 hole

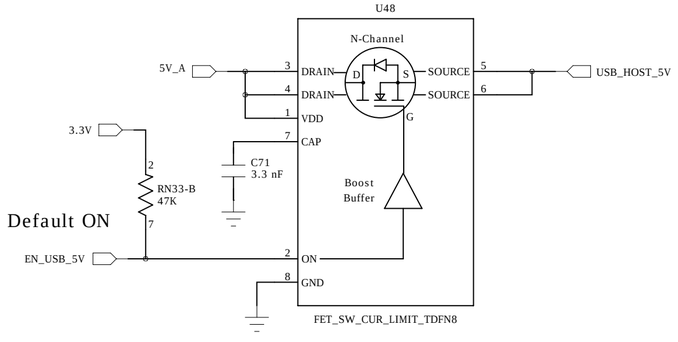
GND

Main 5V Power Sw.



Rise time = 3.5V/ms

USB Sw. 5V



Rise time = 3.5V/ms

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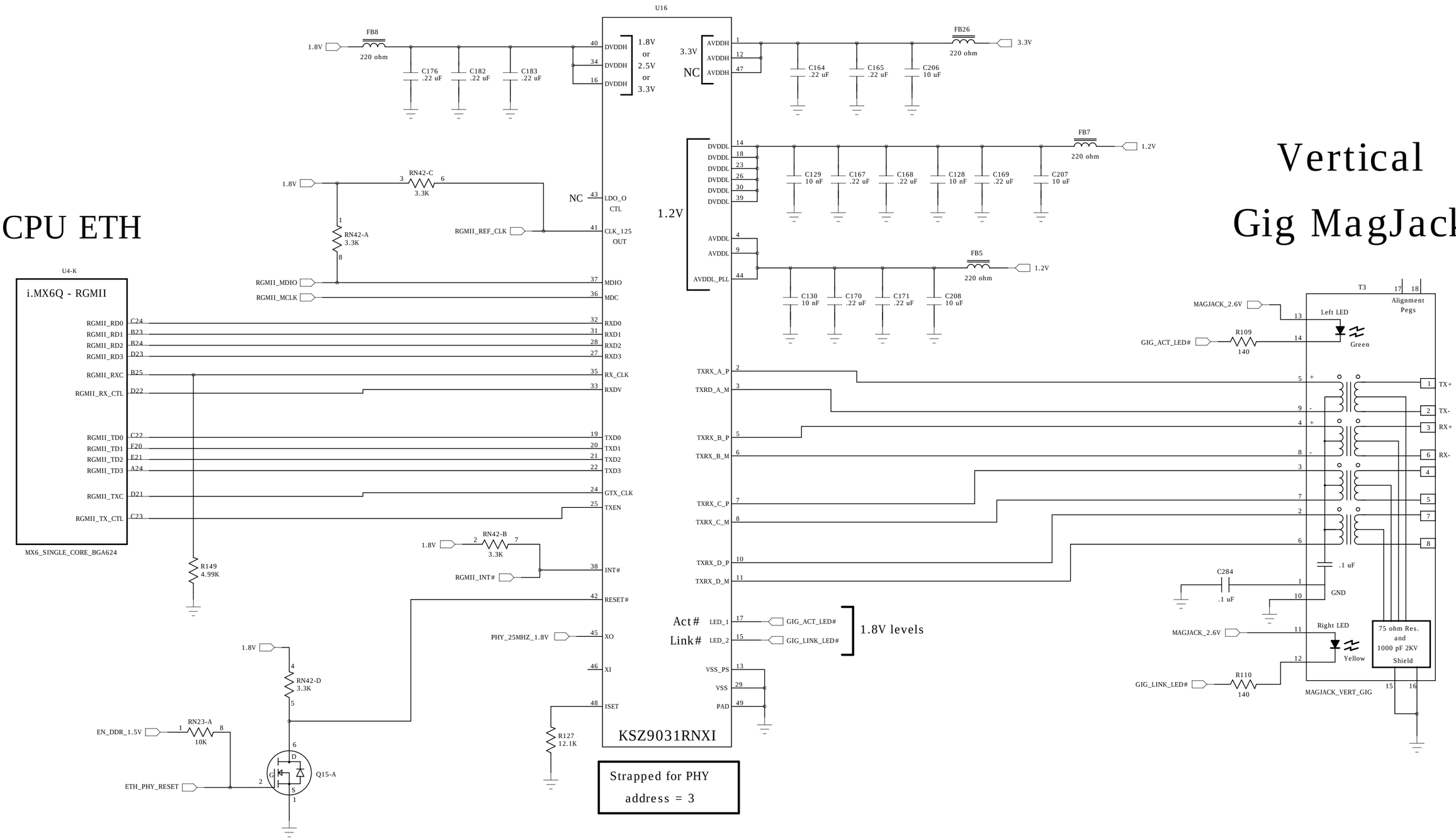
10/100/1000 Ethernet PHY

ETH PHY

CPU ETH

Vertical Gig MagJack



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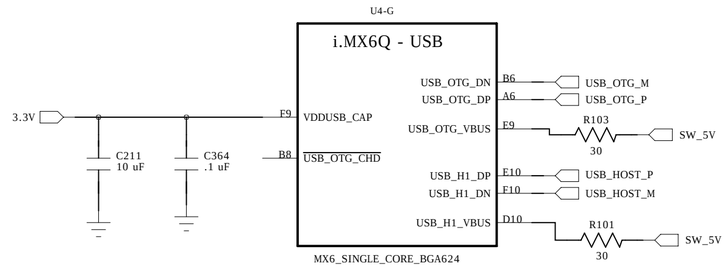
PCIe

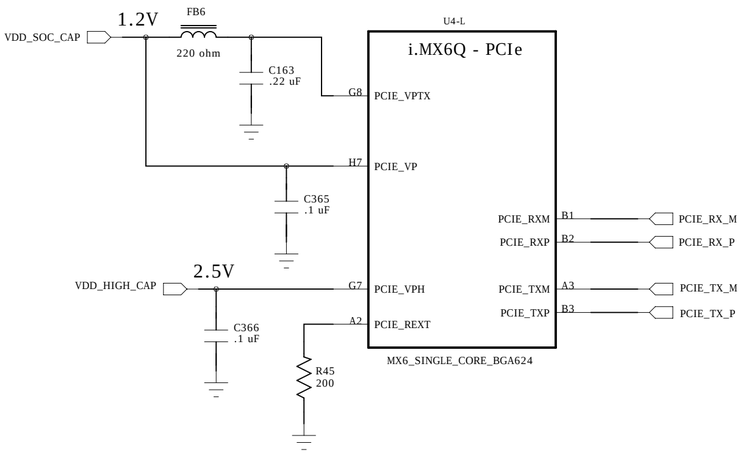
"M" and "P" can be swapped

But "TX" and "RX" can not

CPU USB



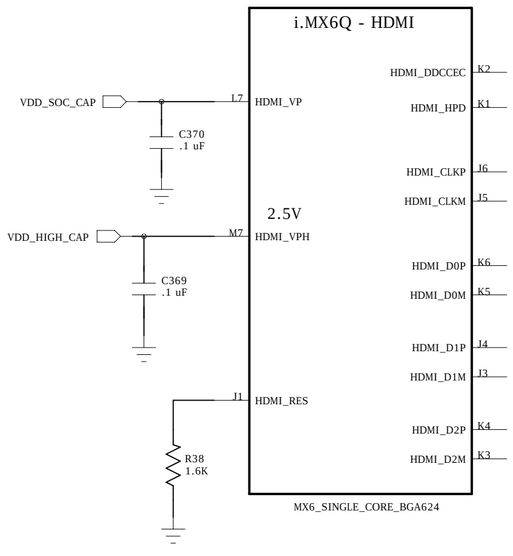
CPU PCIe



PCIe Diff Pairs can be
Polarity swapped

SATA and PCIe Diff pairs do
NOT have to be length matched

CPU HDMI



CEC is a optional
Remote Control

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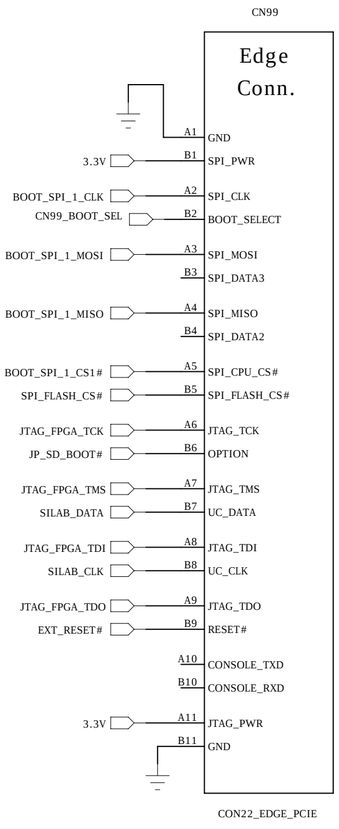
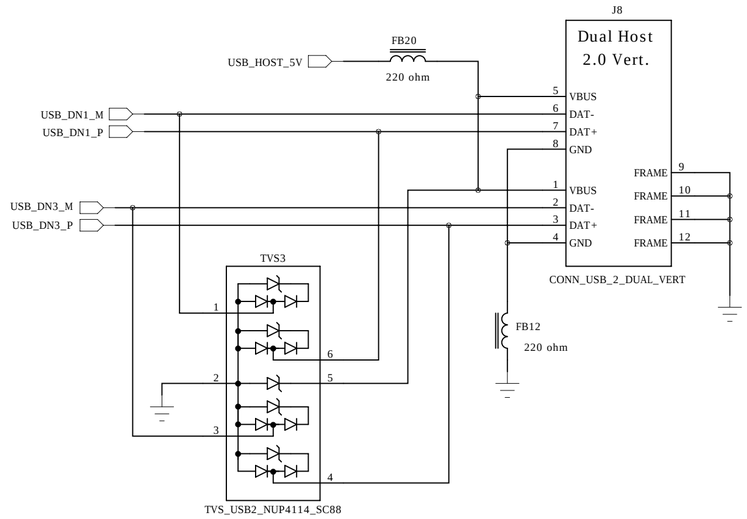
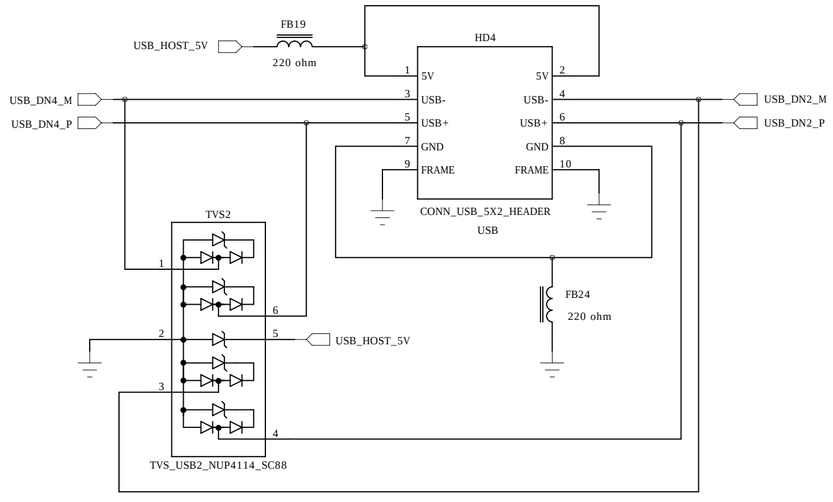
CN99 Programmer Edge Conn.



USB Host Vert. Ports



2x Internal USB Headers



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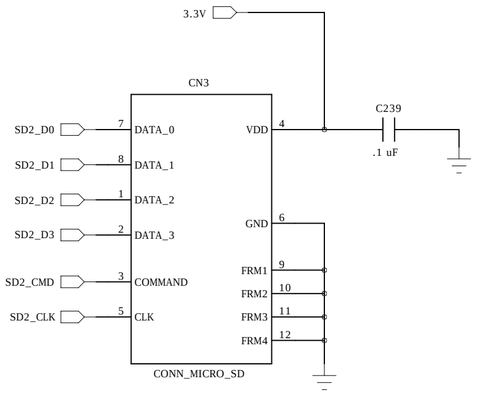
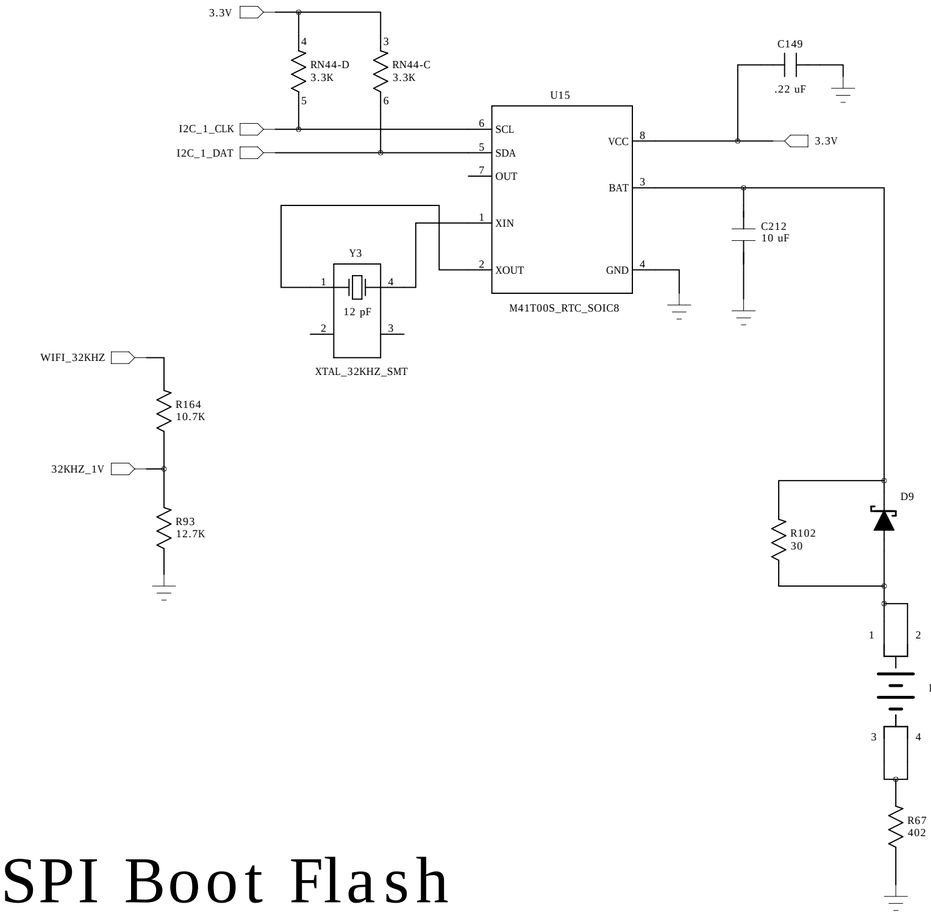
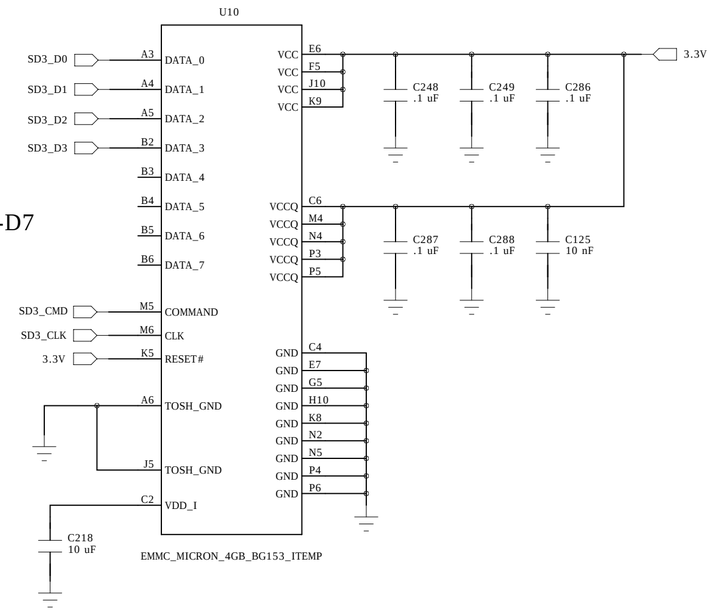
Micro SD Card Socket



ST Micro RTC

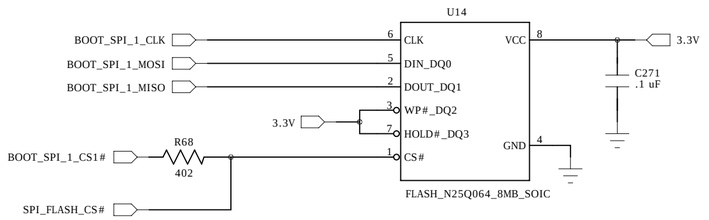


eMMC 4GB



Internal PU on D4-D7

SPI Boot Flash



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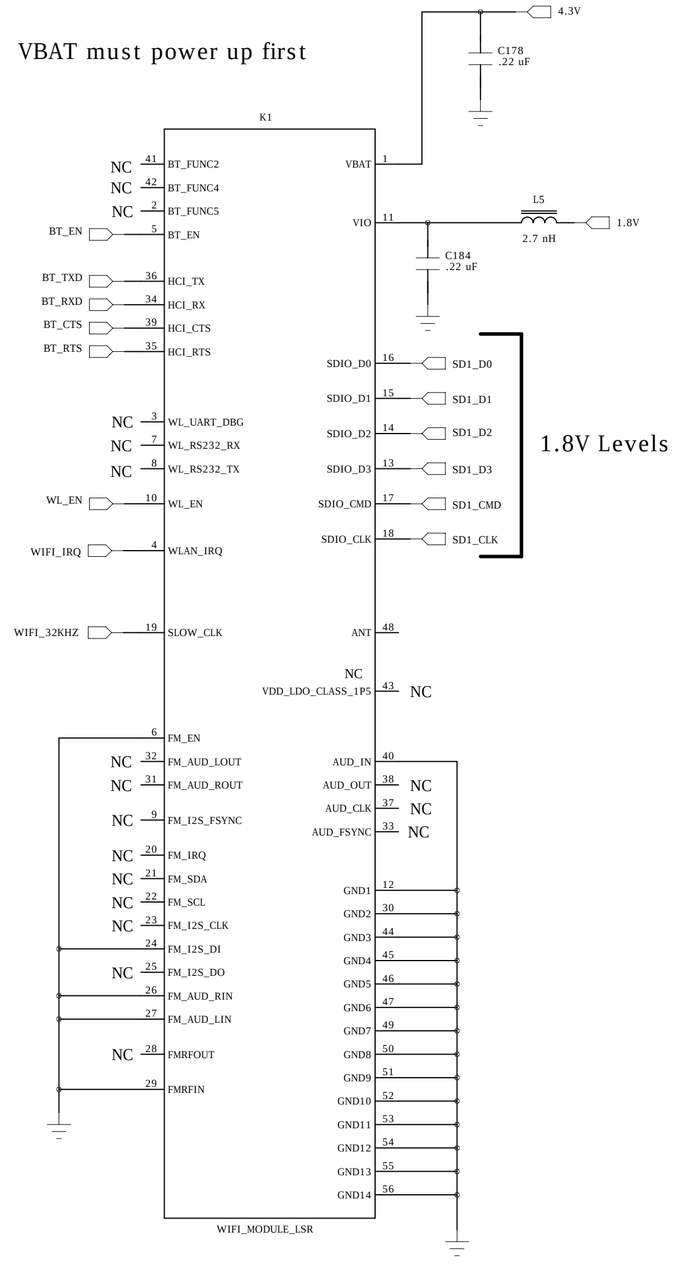
WiFi Radio



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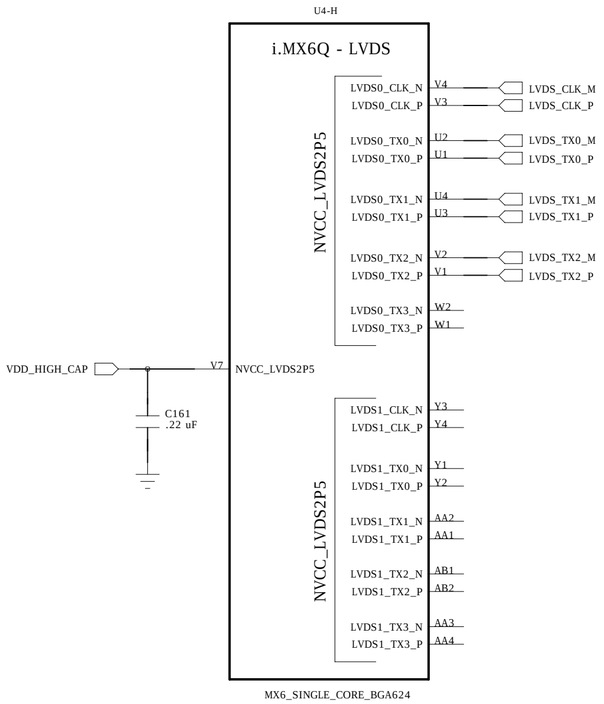
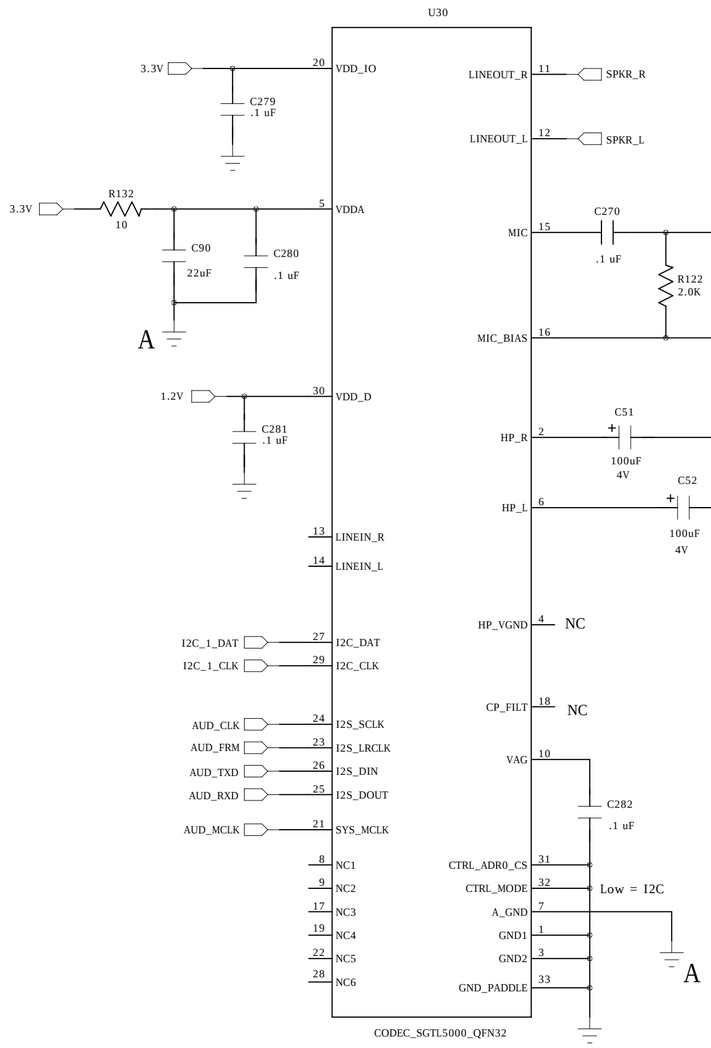
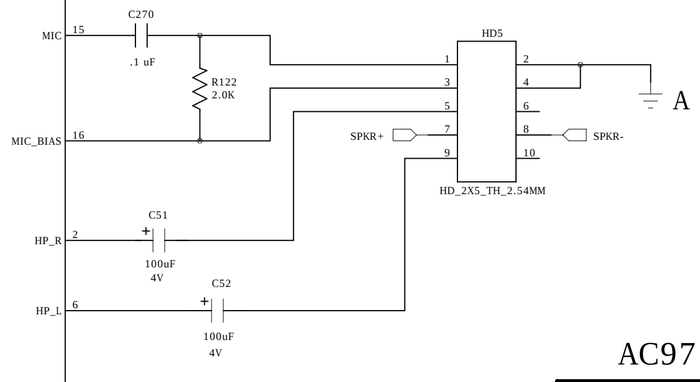
LVDS



Audio CODEC



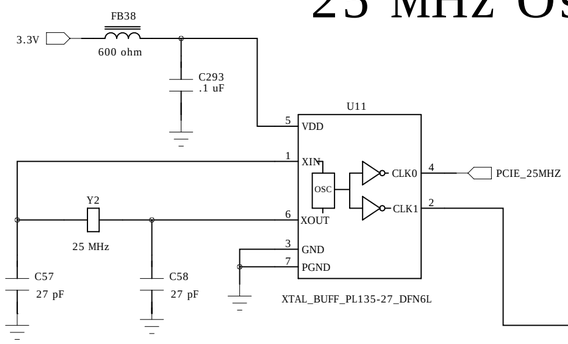
Audio



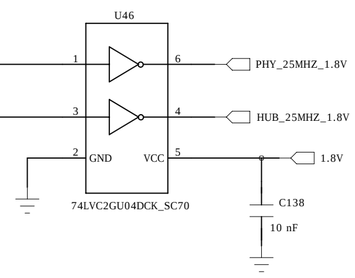
AC97

1) MIC
2) AUD GND
3) MIC Bias
4) AUD GND
5) HP Right
6) HP Right Return
7) AUD 5V or NC
8) Key
9) HP Left
10) HP Left Return

25 MHz Osc.



Level Shifter



Connect AGND to
GND at a single point

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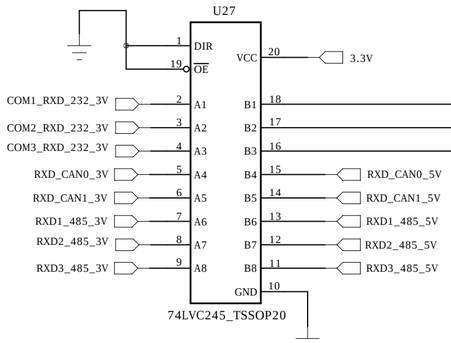
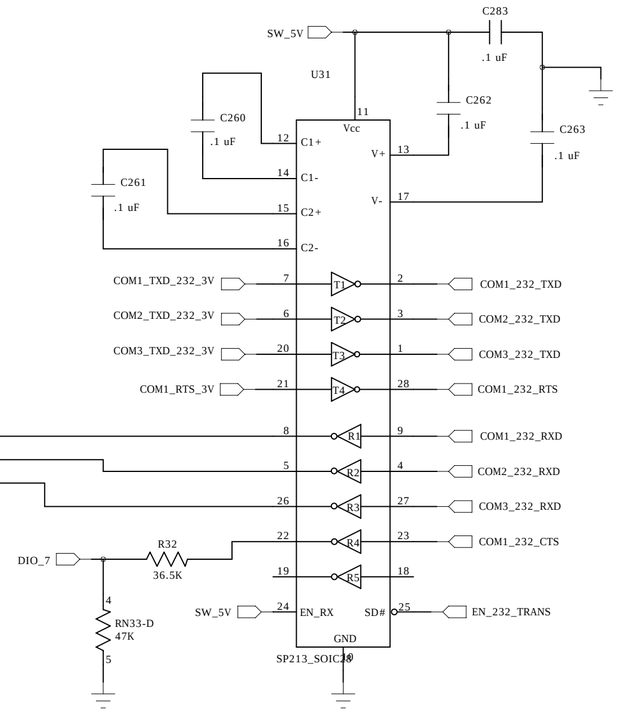
RS-232 Transceiver and COM Headers

3.3V <-- 5V

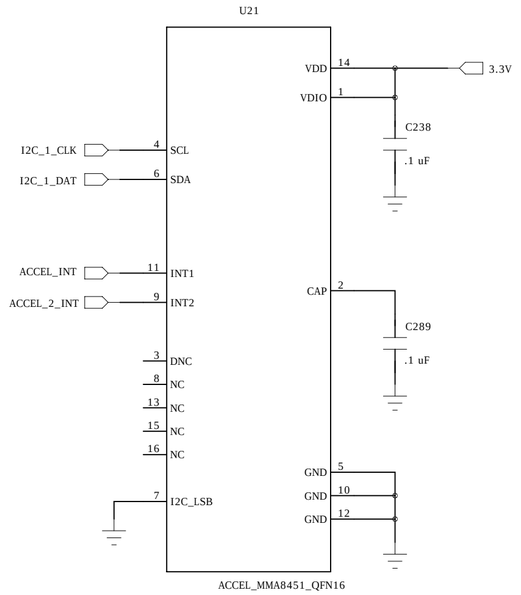
Level shifter



RS-232 Transceiver

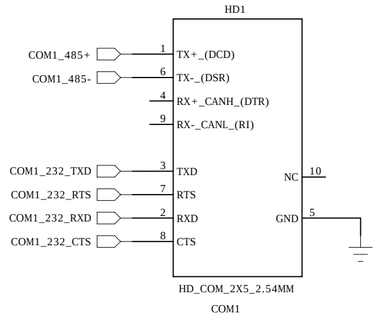


Accelerometer



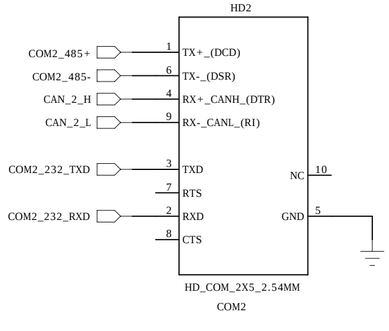
COM1

Header



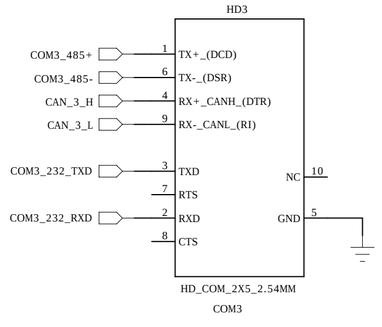
COM2

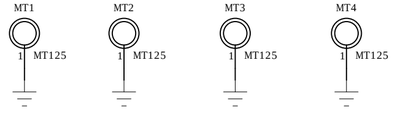
Header



COM3

Header





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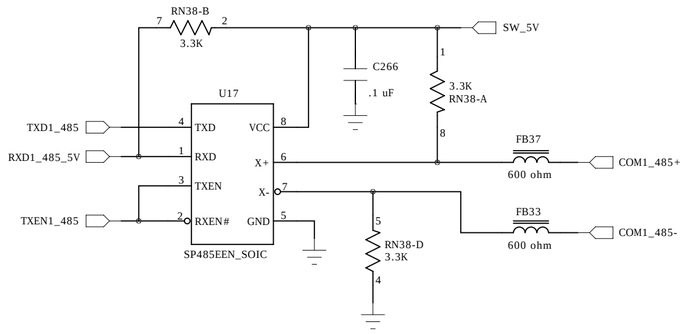
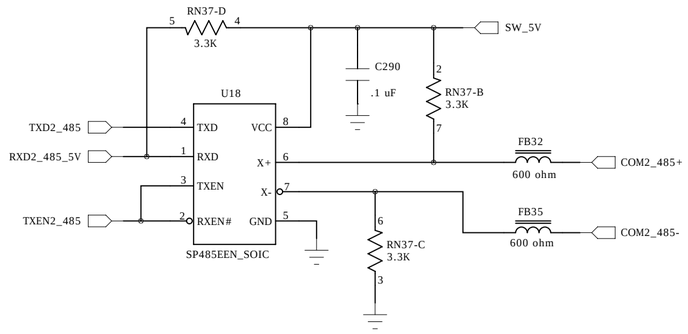
RS-485 and CAN Transceivers

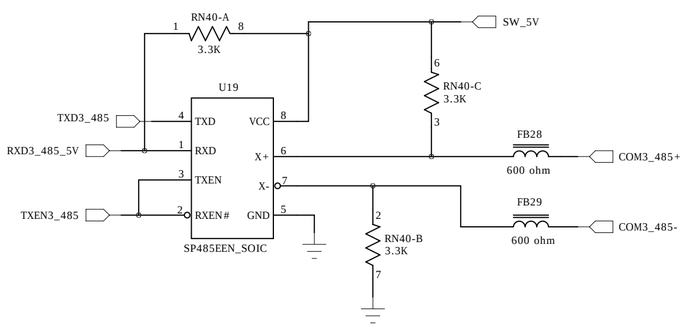
COM1
RS-485 Driver



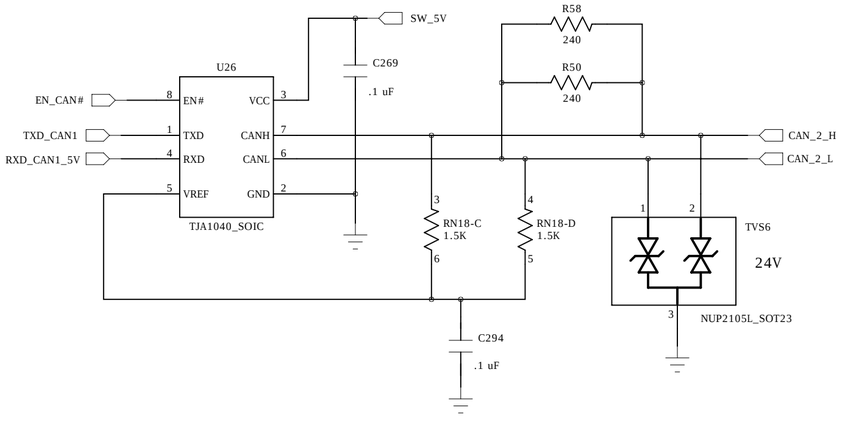
COM2
RS-485 Driver



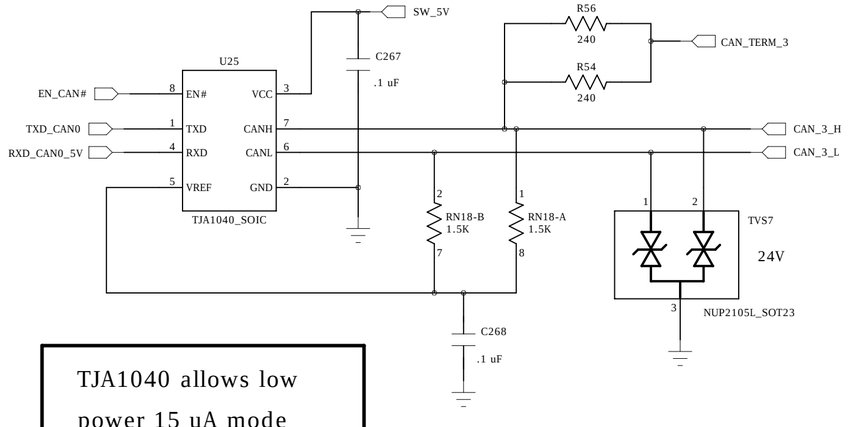
COM3
RS-485 Driver



COM2
CAN Tranceiver



COM3
CAN Tranceiver



TJA1040 allows low power 15 uA mode

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MACH XO2 FPGA

FPGA required for:

- Adds two MAX3100 UART via SPI
- Auto-485 for 3 UARTs
- Provides serial port MUXing
- Level shifting for Bluetooth
- Controls LCD power sequencing
- Option strap resistors
- DIO for DC

CN99_BOOT_SEL must be tri-stated at reset
iMX6 can change it to active high or low

UART2_RTS# needs FPGA PD

R34 pop when WiFi is

R36 and R37
indicate CPU type

R151 thru R153 pop for LXD LCD

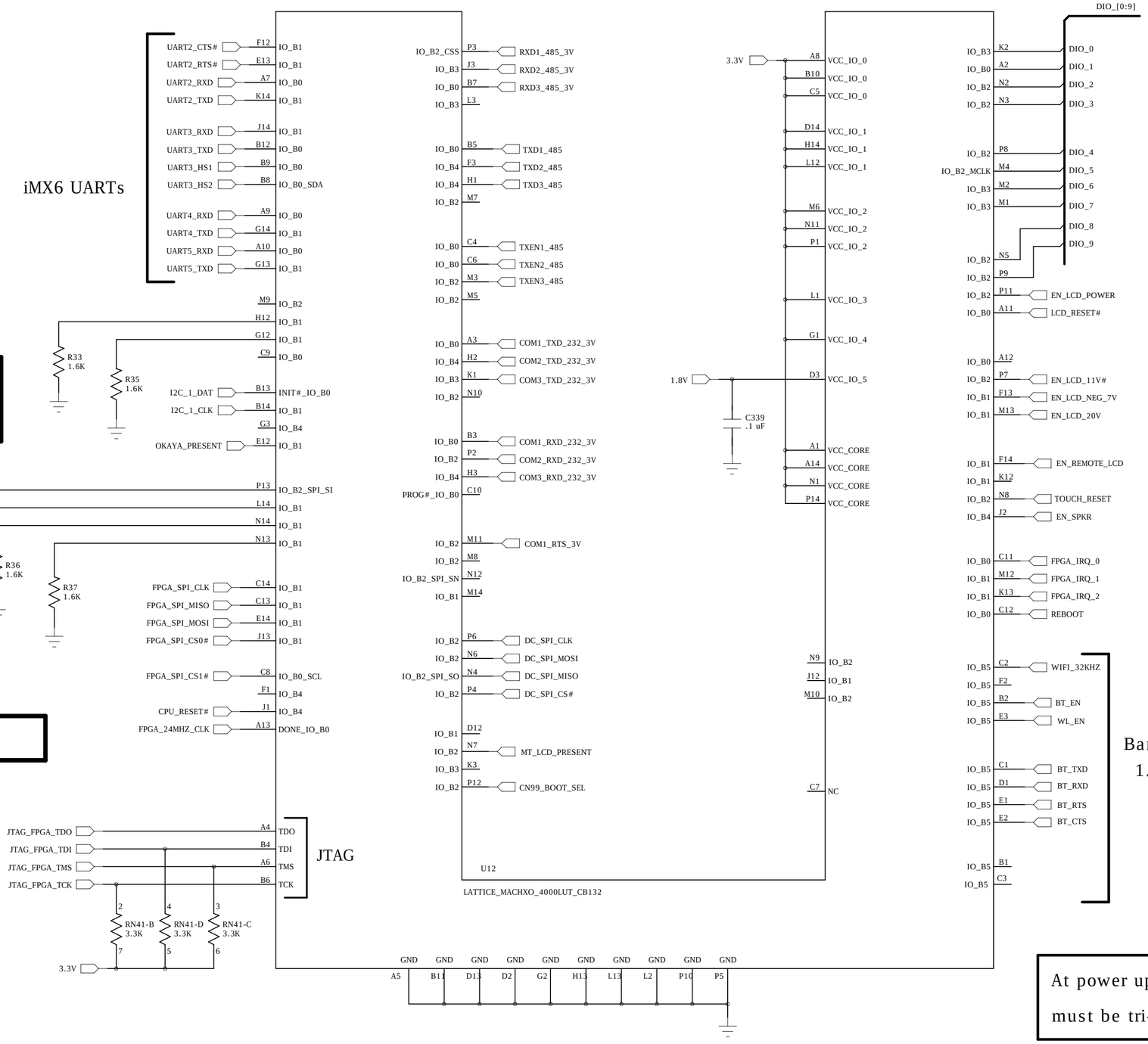
Both MT and LXD LCD conn.
can not be populated, so
strap resistors works well

FPGA ball P13 is high
for MT LCD mode true

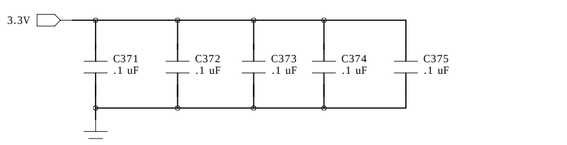
Then FPGA must drive
"MT_LCD_PRESENT" true
only if OKAYA_PRESENT is not true

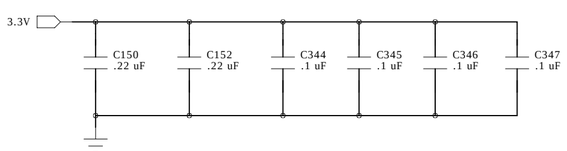
R36 installed = Quad Core

iMX6 UARTs



At power up, all DIO
must be tri-stated





FPGA Features:

- Programmable PU or PD on each pin.
- Internal 2 MHz clock; 10 MHz min PLL clock
- special function pins are in unpredicatble states the 1st 1 ms
- All DIO have Hysteresis inputs

LCD_PWM# is active low
when CPU_PWM is high
Hi-Z when CPU_PWM is low

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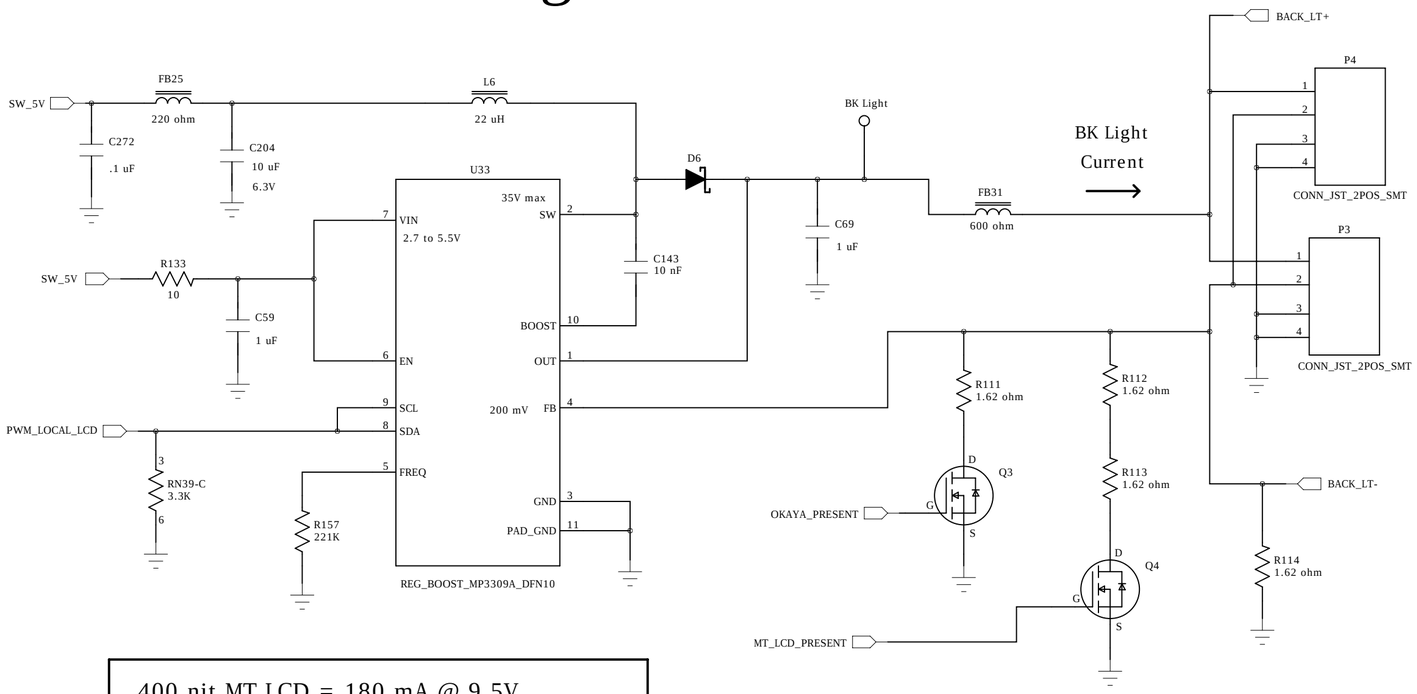
LCD BackLight Power

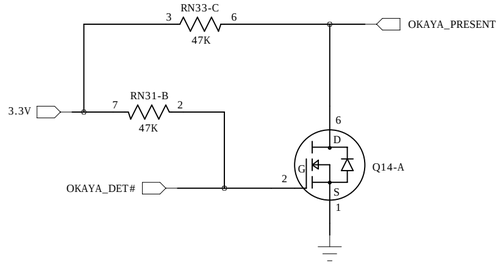


400 nit MT LCD = 180 mA @ 9.5V

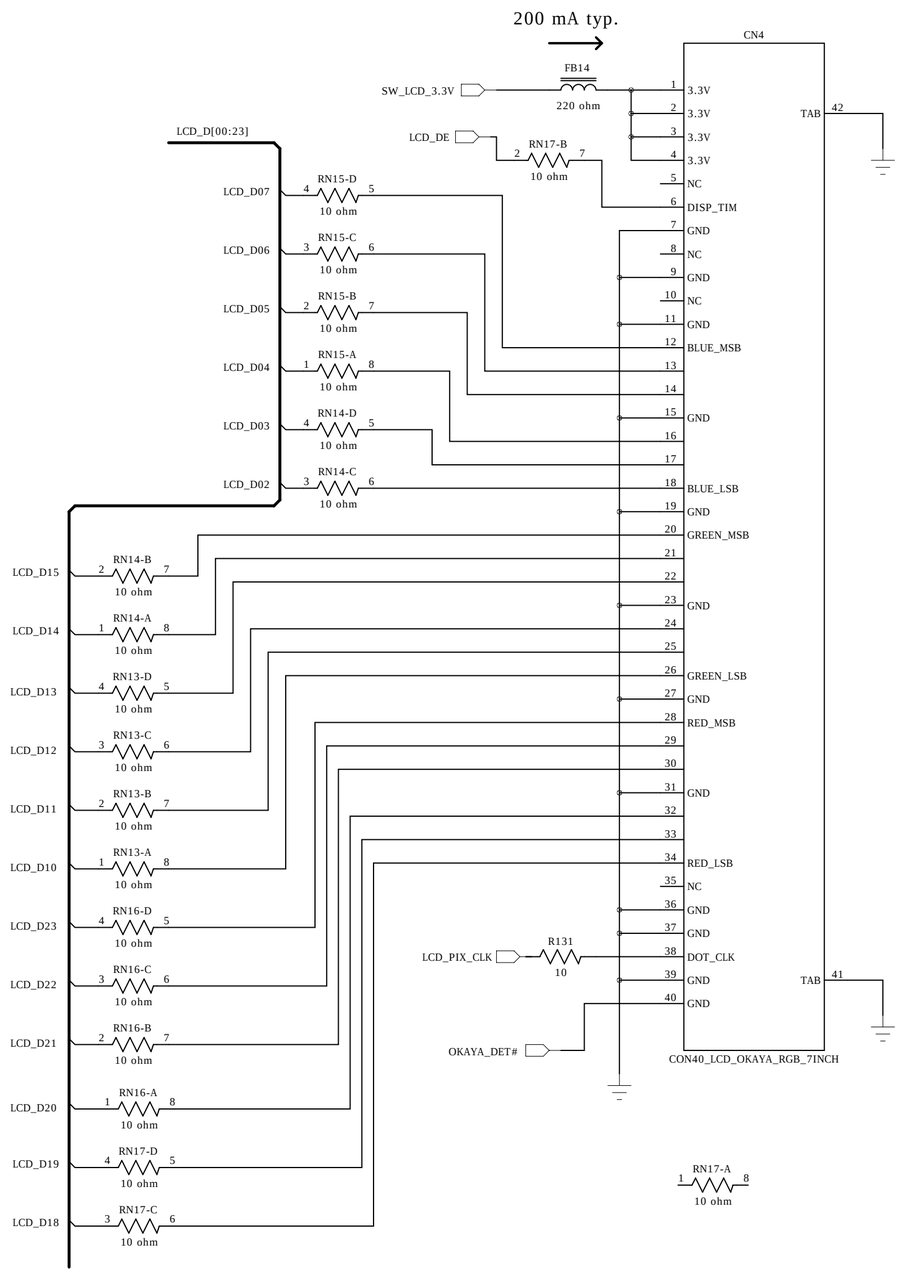
800 nit Okaya = 260 mA @ 10V

800 nit LXD PCAP = 120 mA @ 28V

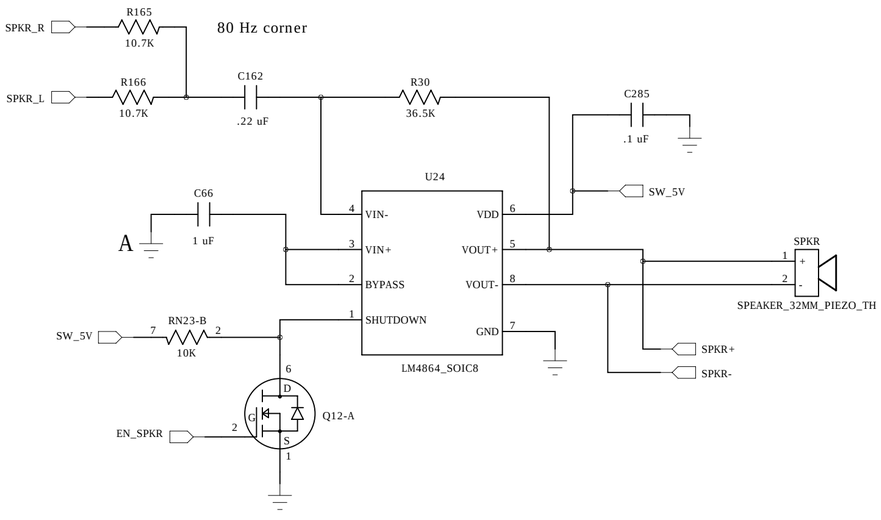
Voltages at LCD terminals



Okaya LCD Conn.



Speaker Amp



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LVDS LCD Conn. LCD

LXD Power Rail Specs

3.3V Rail = 3.3V +-0.3V, Load = 50 mA

Neg 7V = -6.8V +- 0.4V, Load = 1 mA

20V Rail = 20V +- 0.3V, Load = 1 mA

11V Rail = 11.0V +-0.2V, Load = 20 mA

LXD Power up Sequence

Enable LCD Power rails

Wait 50+ ms, deassert LCD_RESET#

Wait 20 ms and turn on 11V

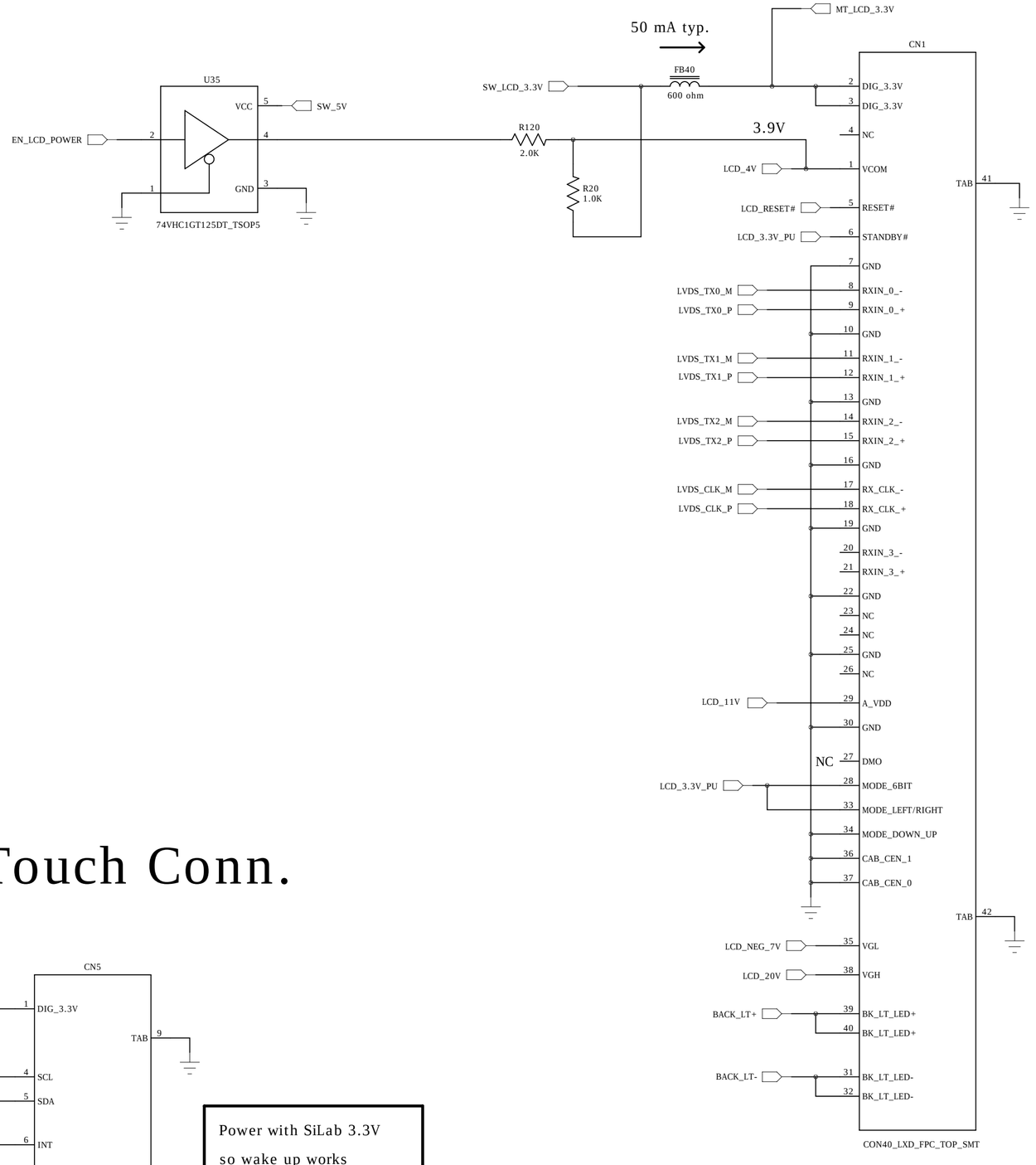
Wait 20 ms and turn on -7V

Wait 30 ms and turn on 20V

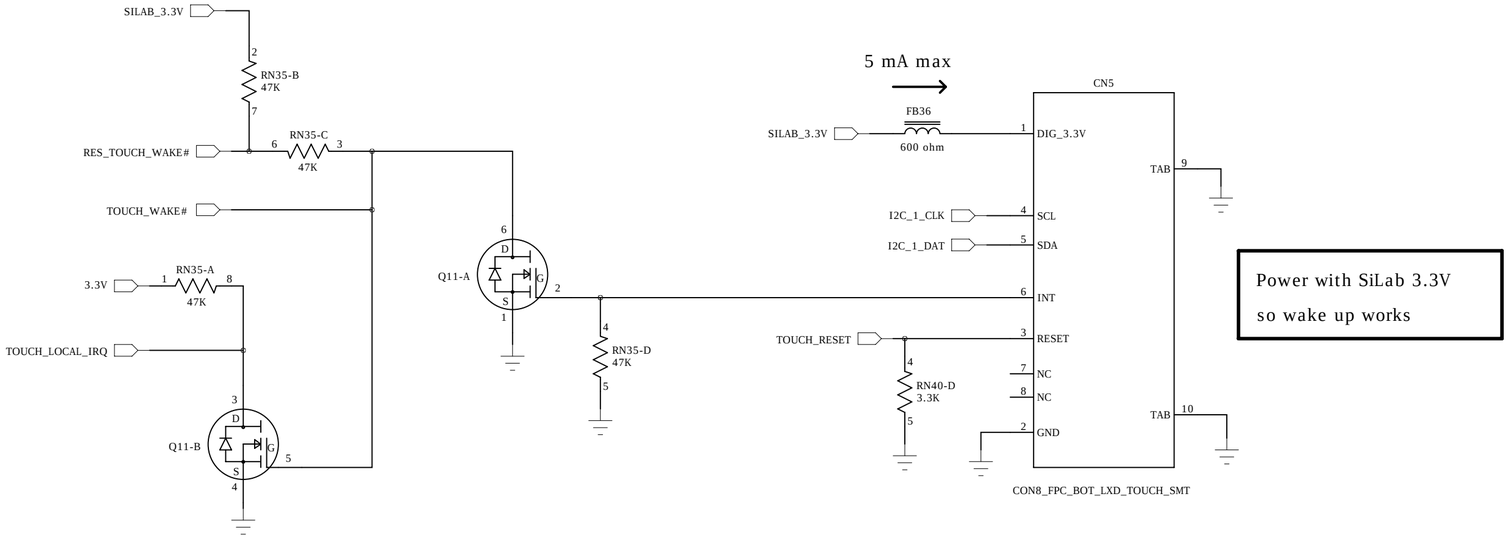
Wait 20ms, Enable LCD Backlite

Wait >10 ms before driving digital inputs

LXD LCD Conn.



LXD Cap. Touch Conn.



Power with SiLab 3.3V
so wake up works

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LXD and MT LCD Power Rails

LXD Power Rail Specs

3.3V Rail = 3.3V +-0.3V, Load = 50 mA

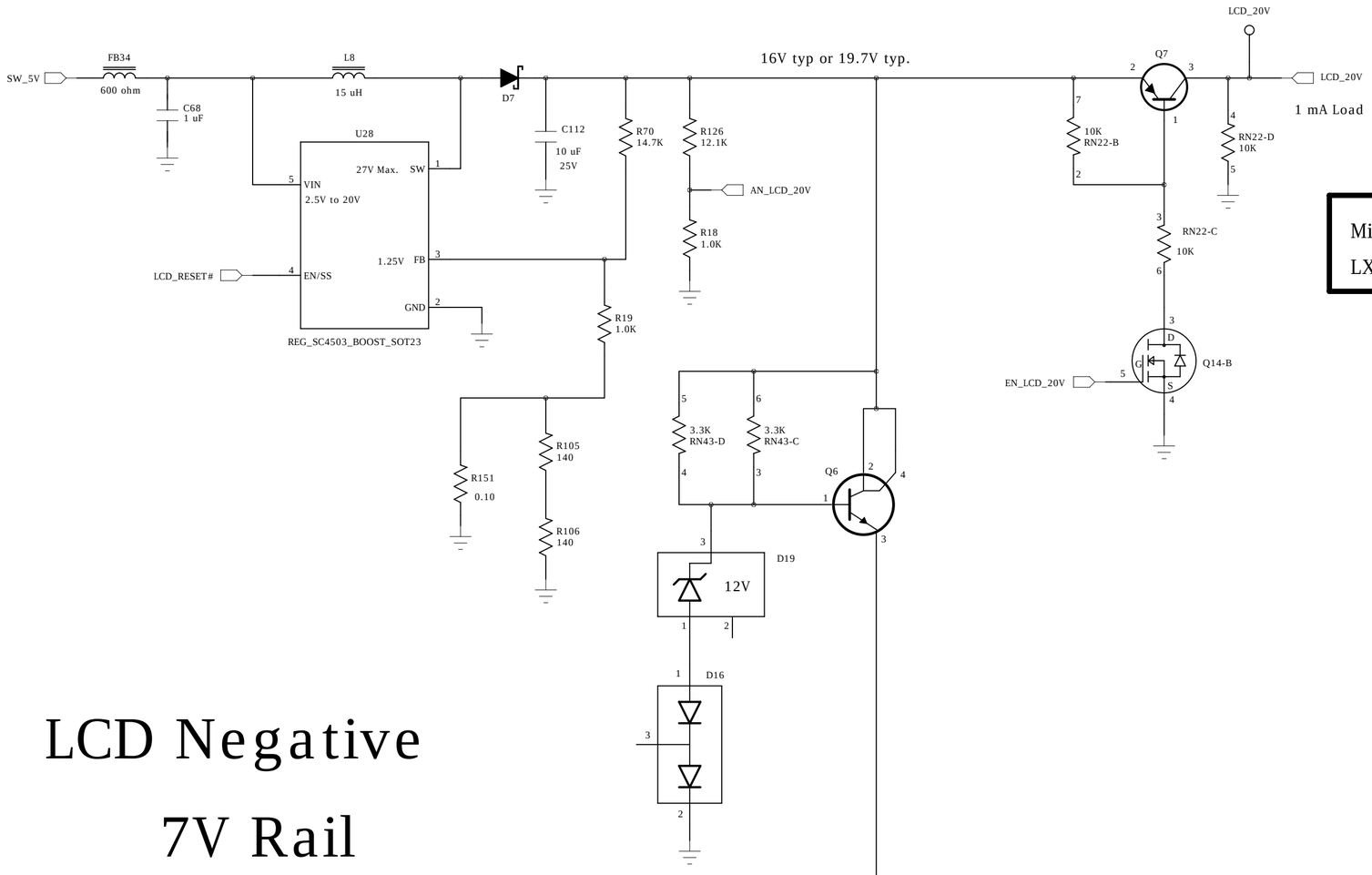
Neg 7V = -6.8V +- 0.4V, Load = 1 mA

20V Rail = 20V +- 0.3V, Load = 1 mA

11V Rail = 11.0V +-0.2V, Load = 20 mA

VCOM = 3.7V +- 1.0V, Load = unknown

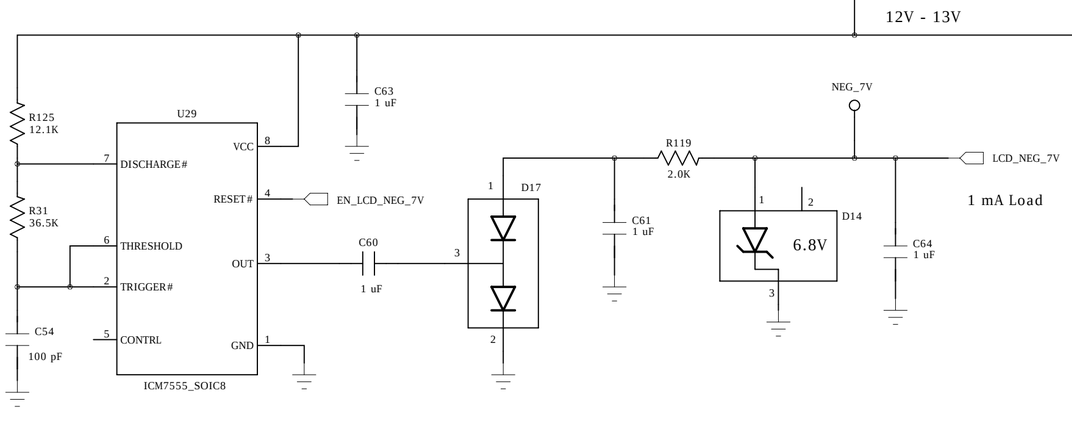
LCD +20V Power Supply



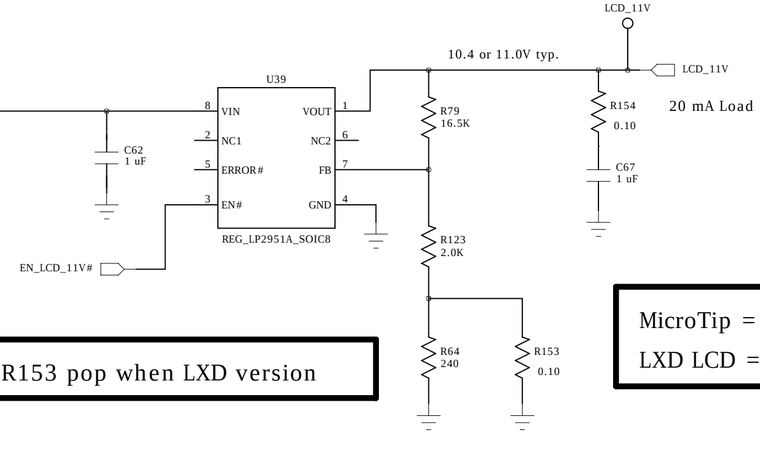
MicroTip = 16.0V

LXD LCD = 20V

LCD Negative 7V Rail



LCD 11V Power Supply



R153 pop when LXD version

MicroTip = 10.4V

LXD LCD = 11V

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MicroTips

LCD Power up Sequence

Assert EN_LCD_POWER true

Wait 50 ms and deassert LCD_RESET#

Wait >20 ms and turn on -7V

Wait >5 ms and turn on 11V (10.4V)

Wait >5 ms and turn on 20V (16V)

Wait >20 ms, turn on LCD backlight

Wait >10 ms before driving digital inputs

MicroTips

LCD Power Rail Specs

3.3V Rail = 3.0 to 3.6, Load = 10 mA

Neg 7V = -7.7V to -6.3V, Load = 1 mA

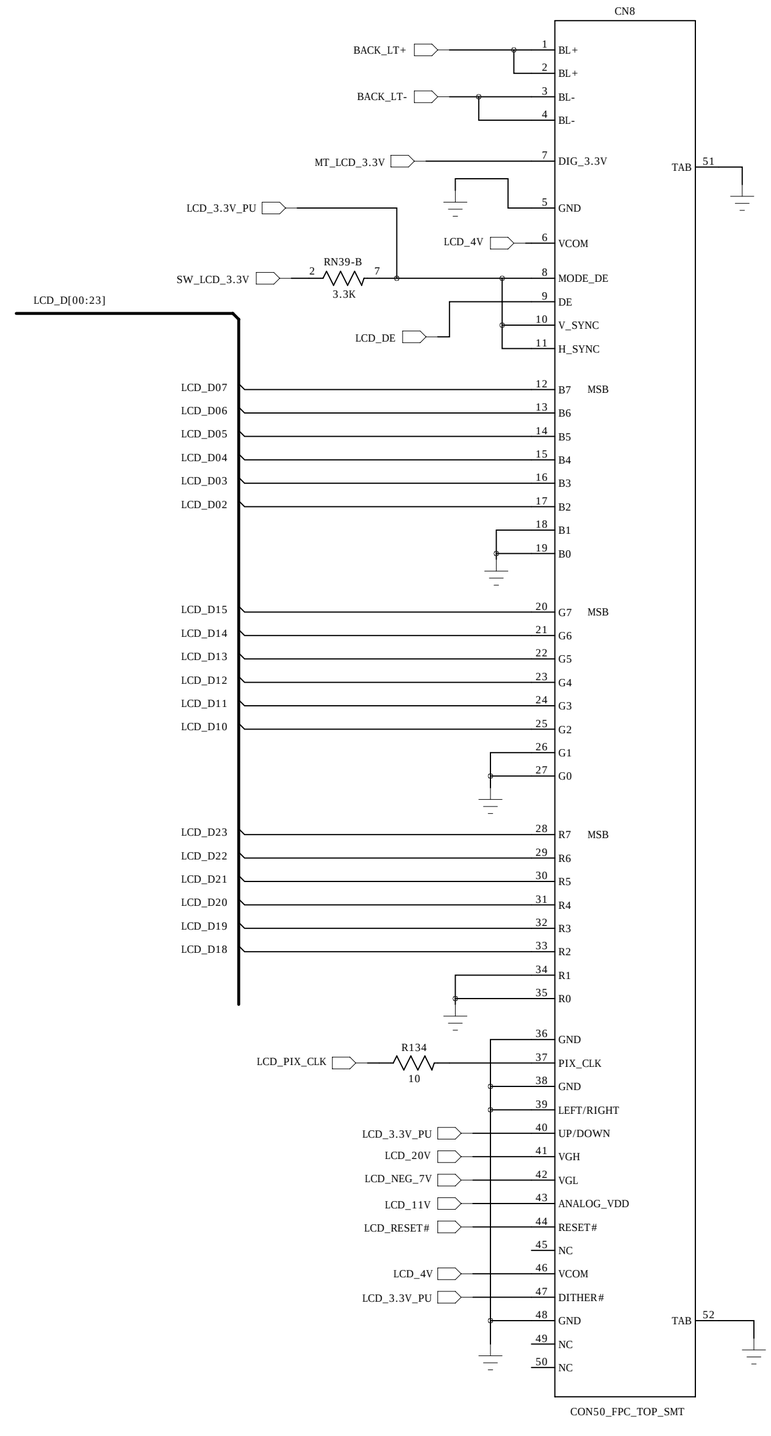
16V Rail = 15.3V to 16.7V, Load = 1 mA

10.4V Rail = 10.2 to 10.6, Load = 20-30 mA

VCOM = 4.0V +/- 0.2V, Load = unknown

MicroTips

LCD Conn.



Top Contacts

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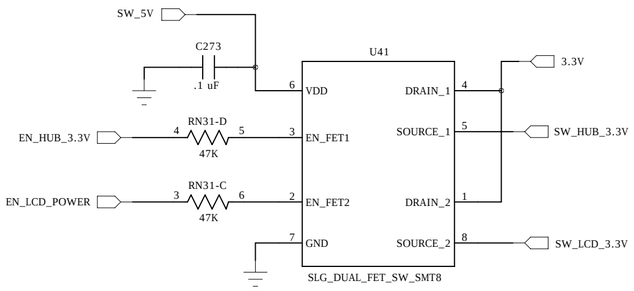
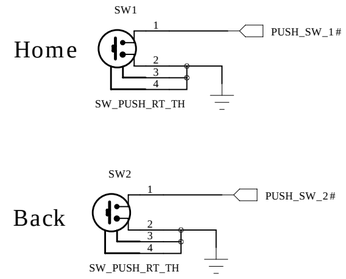
LCD Res. Touch

Hub and LCD Power Switch



Rise time of both outputs measured at ~1V/ms

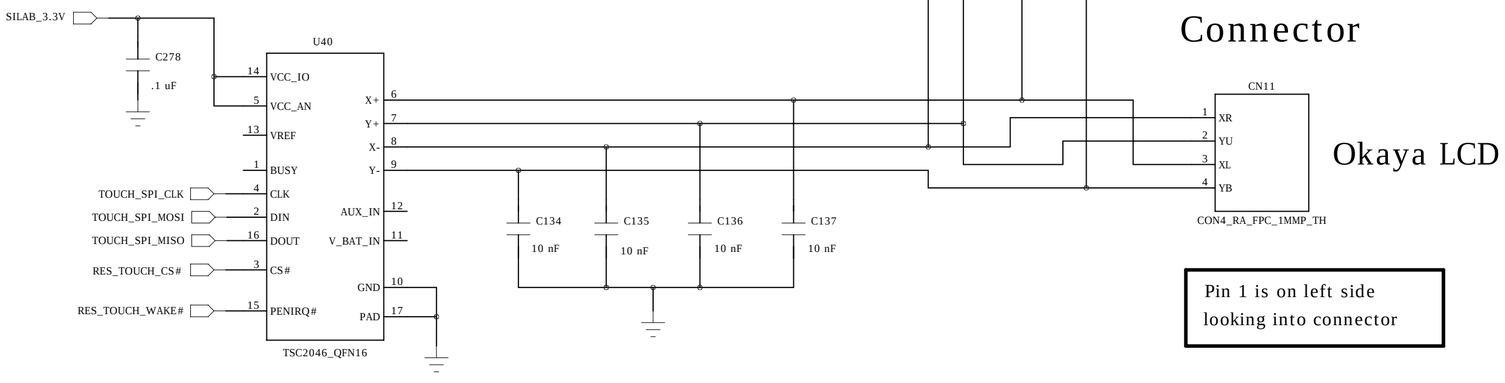
Android Push Switches



LXD Power up Sequence

Enable LCD Power rails
Deassert STBY# at the same time
Wait 50+ ms, deassert LCD_RESET#
Wait 20 ms and turn on 11V
Wait 20 ms and turn on -7V
Wait 30 ms and turn on 20V
Wait 20ms, Enable LCD Backlite
Wait >10 ms before driving digital inputs

Resistive Touch Screen Controller



Pin 1 is on left side looking into connector

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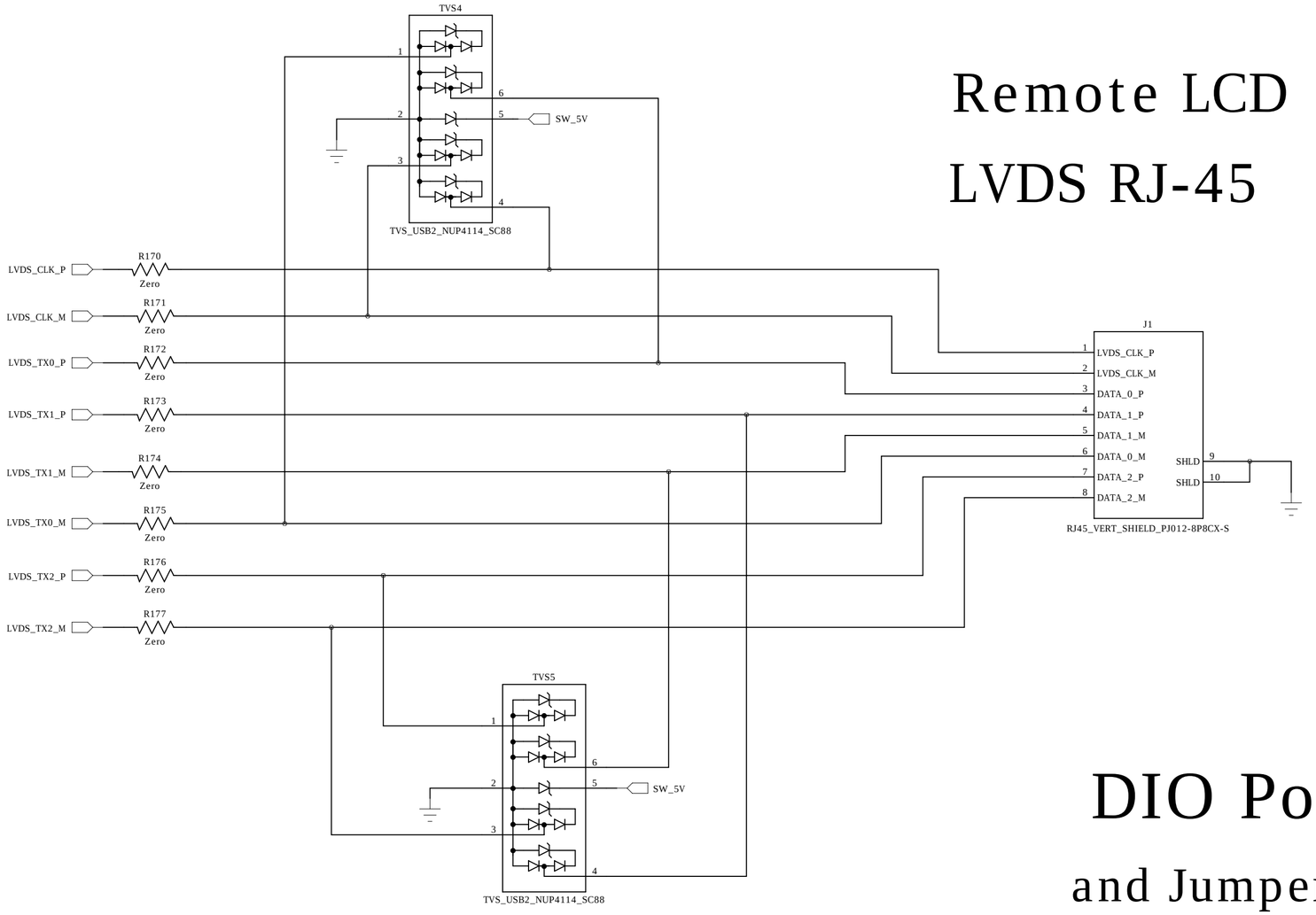
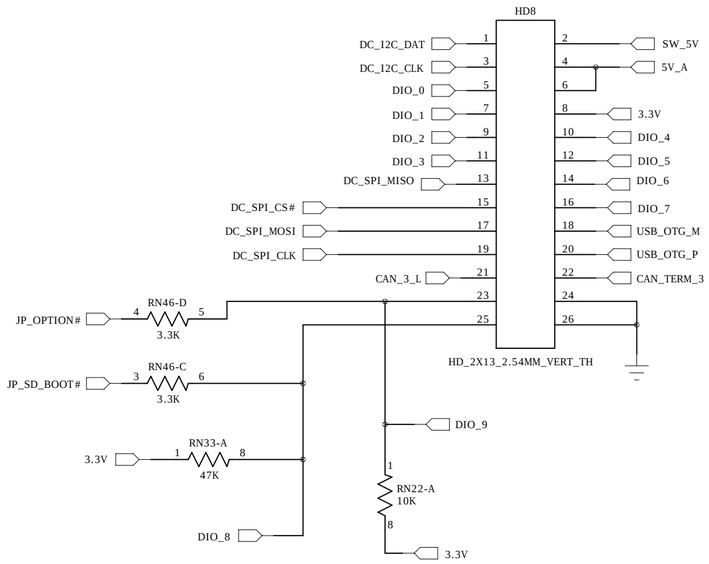
LVDS Diff pairs need
to be length matched

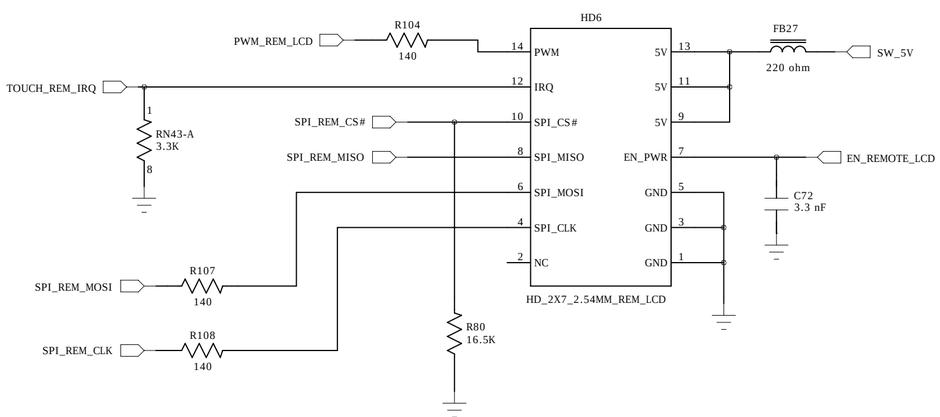
Remote LCD
LVDS RJ-45



DIO Port
and Jumpers



Remote LCD
2x7 Header



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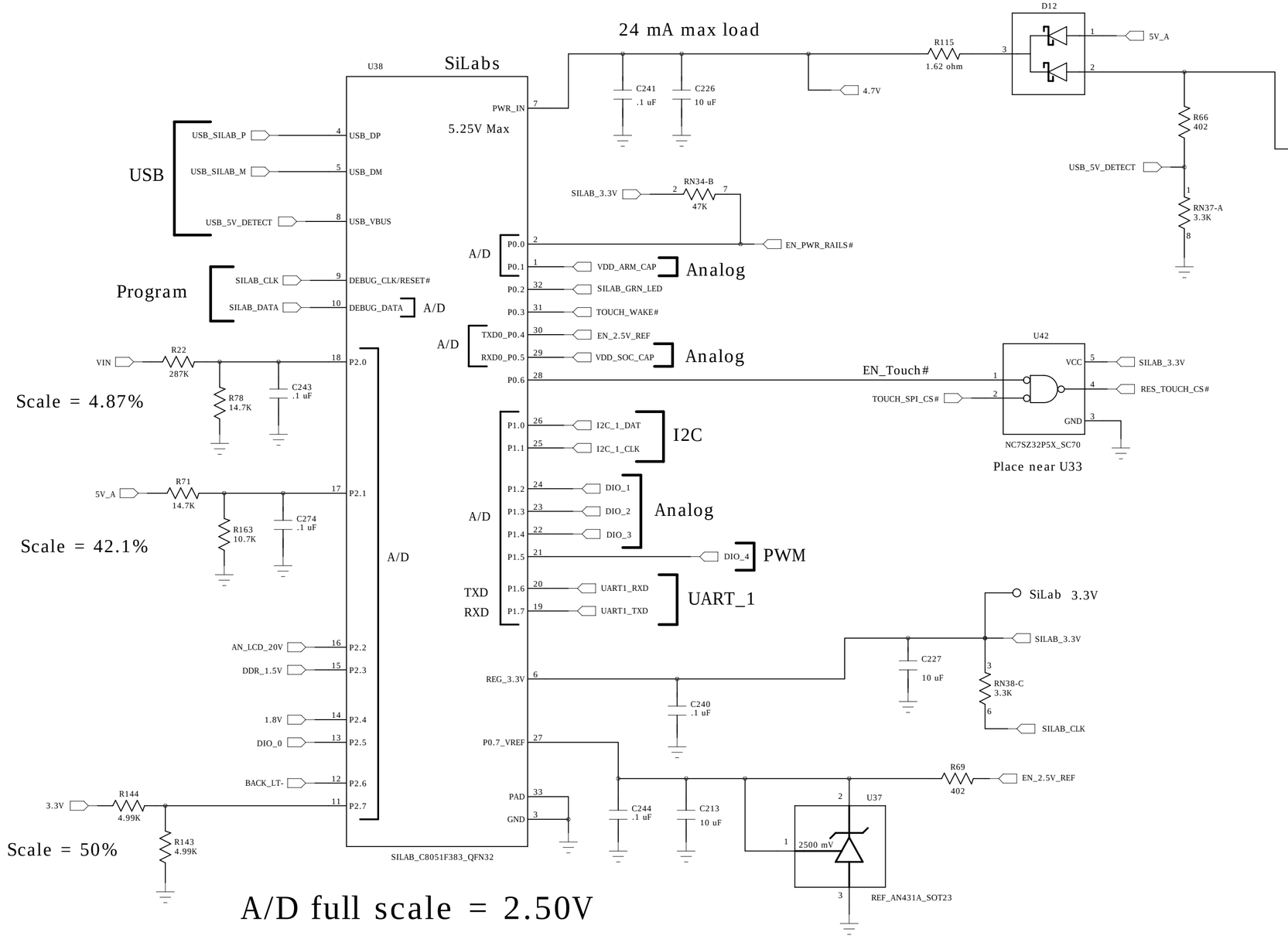
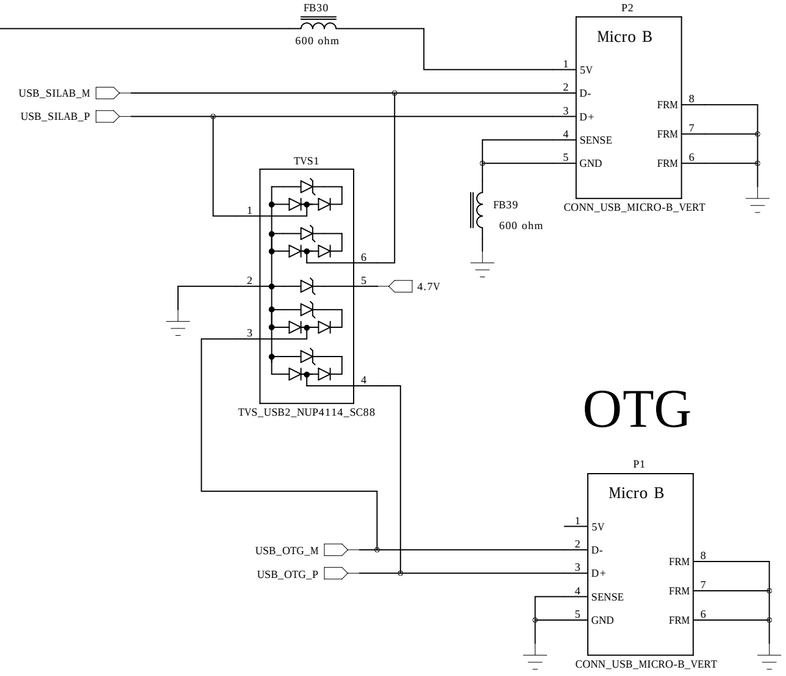
USB Device Port and Silab uC

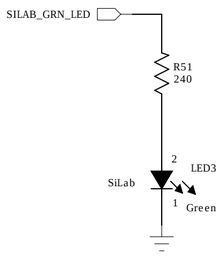


USB Device Port



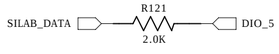
OTG

SiLab LED



Power Hold Circuit

- DIO_0 = Analog CHRG_V
- DIO_1 = SuperCap1_V
- DIO_2 = SuperCap2_V
- DIO_3 = V_Internal
- DIO_4 = PWM
- DIO_5 = DIO
- DIO_6 = Power Fail



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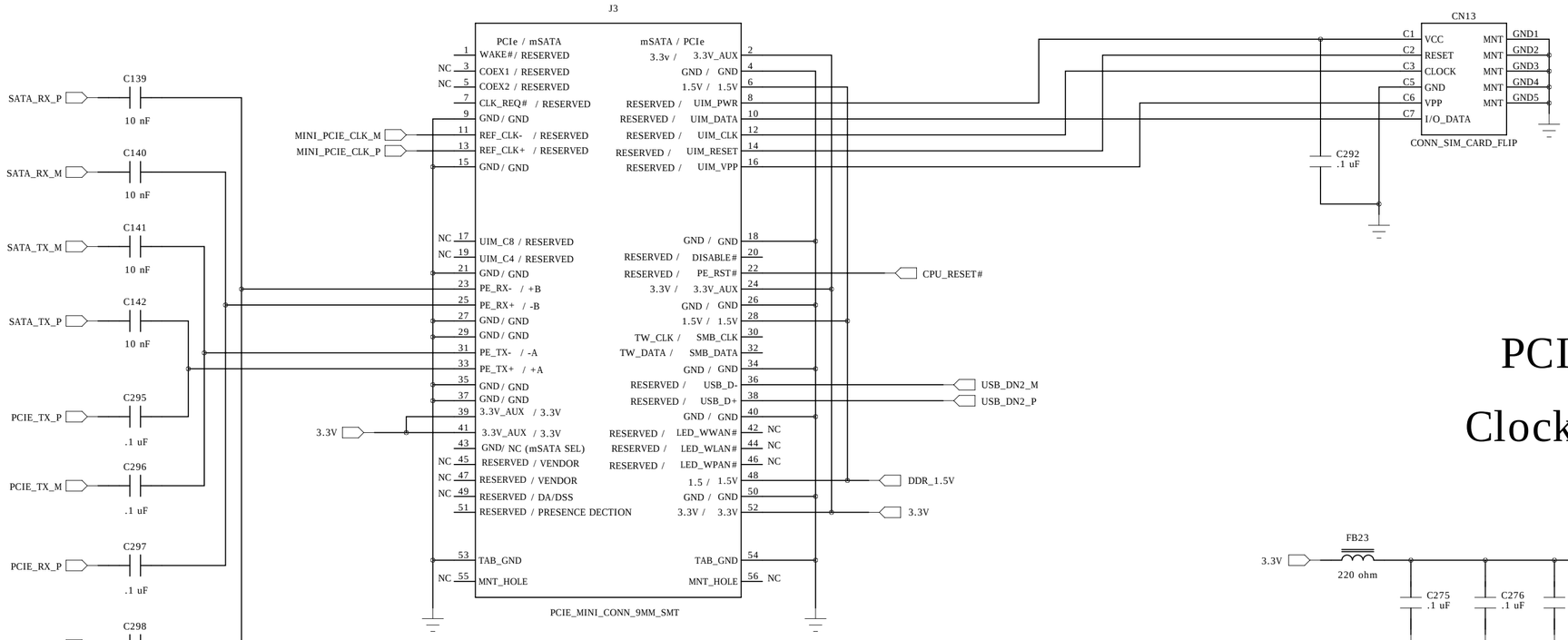
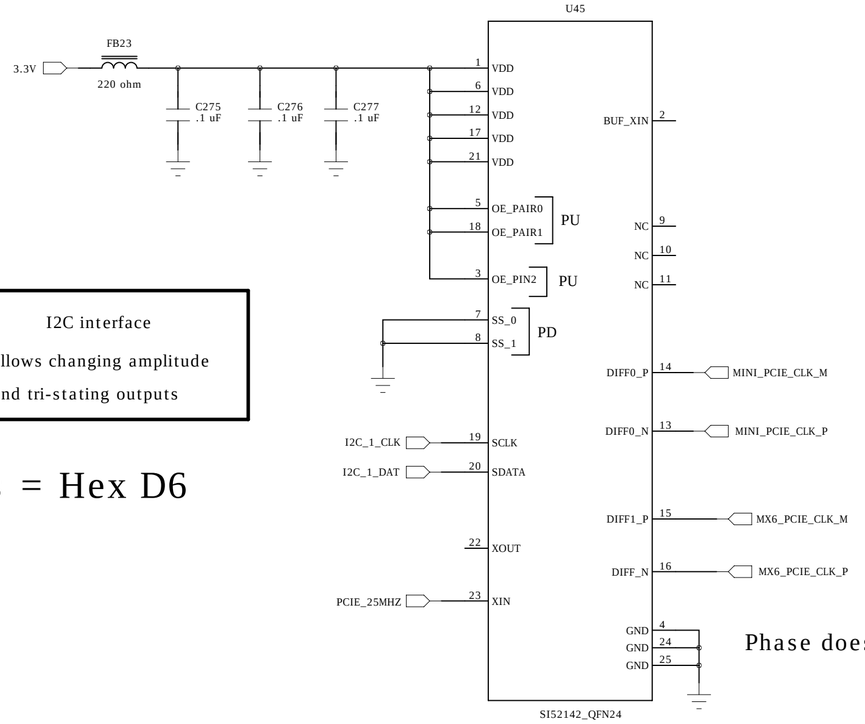
7mm Stack Height to center of bd.

Mini PCIe SIM Card Connector



PCIe 100 MHz Clock Generator

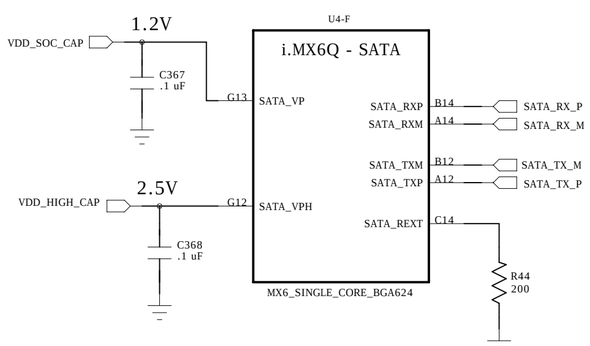


I2C interface
allows changing amplitude
and tri-stating outputs

I2C address = Hex D6

Phase does not matter

SATA



PCIe Diff Pairs can be
Polarity swapped

SATA and PCIe Diff pairs do
NOT have to be length matched

MT5 PEM_6MM_SMT

MT6 PEM_6MM_SMT

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