System Level Block Diagram
TS-7800-V2 Rev A SBC

Marvell Armada 385
Dual Core
1.33 GHz
-40C to +85C

FPGA
20Klut, 145 I/O
-40C to +85C

DDR3 RAM
1GByte
128MByte w/ECC

4GByte
8-64GByte

Micro SD Card Socket
Full Size SD Card Socket

Micro USB Device
(Console)

Battery Holder
RTC

Accelerometer

Spi Labs μC:
System Monitor/
Debug Support/
Temp Sensor

10 bit ADC

5V Level
Shift

SATA
USB2.0
USB3.0
USB2.0
SATA
SATA
SATA
Ethernet

Ethernet PHY
10/100/1000M

RS-232
Transceiver

RS-485
Transceiver

RS-232
Transceiver

RS-232
Transceiver

RS-232
Transceiver

RS-232
Transceiver

2x5 Header:
COM3
RS-232/2x RS-485

DB9: 3x RS-232

Diagnostic
LEDs

UBoot pause
SD Boot
Console

mSATA
miniCard

SRIO

RTC

I2C

SPI

USB3.0
USB2.0

Optimal Feature = (Optional Feature)

4GByte
4-64GByte

eMMC

8V-30V
DC/DC

Regulator

Full Size
SD Card
Socket

5V
Level
Shift

TVS

TVS

TVS

TVS

TVS

TVS

TVS

Console

frm DB9

frm Console

2x3 Header
TS-781

2x5 Header:
A/D
x5 5V Analog In

5V Level
Shift

Input Power
5V
GND

TS-781
8V-30V
DC/DC
Regulator

Micro USB
Device
(Console)

Accelerometer

WiFi
802.11 b/g/n
Bluetooth
BLE Radio

Diagnostic
LEDs

UBoot pause
SD Boot
Console

mSATA
miniCard

SRIO

RTC

I2C

SPI

USB3.0
USB2.0

Optimal Feature = (Optional Feature)